A NOVEL OXIDE VERTICAL MOSFET (OVMOS) TRANSISTOR STRUCTURE

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الخلاصة :

نظراً لما تتطلبه صناعة الدوائر المتكاملة من نبائط عالية الكثافة ، فإنَّ البحث يقدِّم تطويراً لتكوين الترانزستور الرأسي ليشغل مساحة أقل مع الاحتفاظ بكلٍّ من خصائص الانتقال والخرج . ويمتاز الترانزستور الجديد بأنَّ مادة البوليسيليكون التي تتكون منها البوابة تحيط بقناة الترانزستور المطوَّر من جهتين فقط ، وهو ما يحقق زيادة كثافة النبائط .

وقد تَـمَّ تمثيل ومقارنة خاصية الانتقال في كل من الترانزستور الرأسي المطوَّر والترانزستور الأفقي التقليدي ولوحظ تحسن ميل منحنى خاصية الانتقال في نطاق ما قبل التشغيل للترانزستور الرأسي ليساوي ٧٣ ملي ڤولت / وحدة عشرية عند جهد قاعدة = ٥ , ٢ ڤولت . كما يمتاز التكوين الجديد بأنَّ طول قناة التوصيل للترانزستور لا يعتمد على تقنية التصنيع ، وهو ما يحقق أداءً أفضلَ حتى مع تقنيةِ تصنيعٍ متوسطة .

ABSTRACT

A novel high-density oxide vertical MOS (OVMOS) transistor with compact structure has been developed for future MOS devices. This transistor, whose gate electrode surrounds only two sides of the pillar silicon island, reduces the occupied area for all kinds of circuits. More than 70% of the occupied area can be saved with the new structure, which will be suitable for future ULSI's. Other advantages are steep cut-off characteristics (low subthreshold swing S = 73 mV/decade) and small substrate bias effects. Also the channel length of OVMOS is independent on the technology linewidth and high performance could be achieved with OVMOS circuits for any scale of integration.

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1. INTRODUCTION

In order to achieve future VLSI devices with higher packing density, several three-dimensional MOS structures have been proposed [1–6]. However the average device area reduction is still limited due to the required isolation thickness, necessary to avoid the leakage charge between the adjacent transistors. In this paper a novel high density Oxide Vertical MOS (OVMOS) structure is introduced. The OVMOS structure is given in Section 2. The proposed fabrication process steps of the OVMOS structure are given in Section 3. The OVMOS structure has been simulated using the device simulator PISCES-IIb [7], and the simulation results are given in Section 4. Conclusion is given in Section 5.

2. OVMOS DEVICE STRUCTURE

The structure of OVMOS transistor (top view and cross section) is shown in Figure 1. The significant feature of such a structure is that:

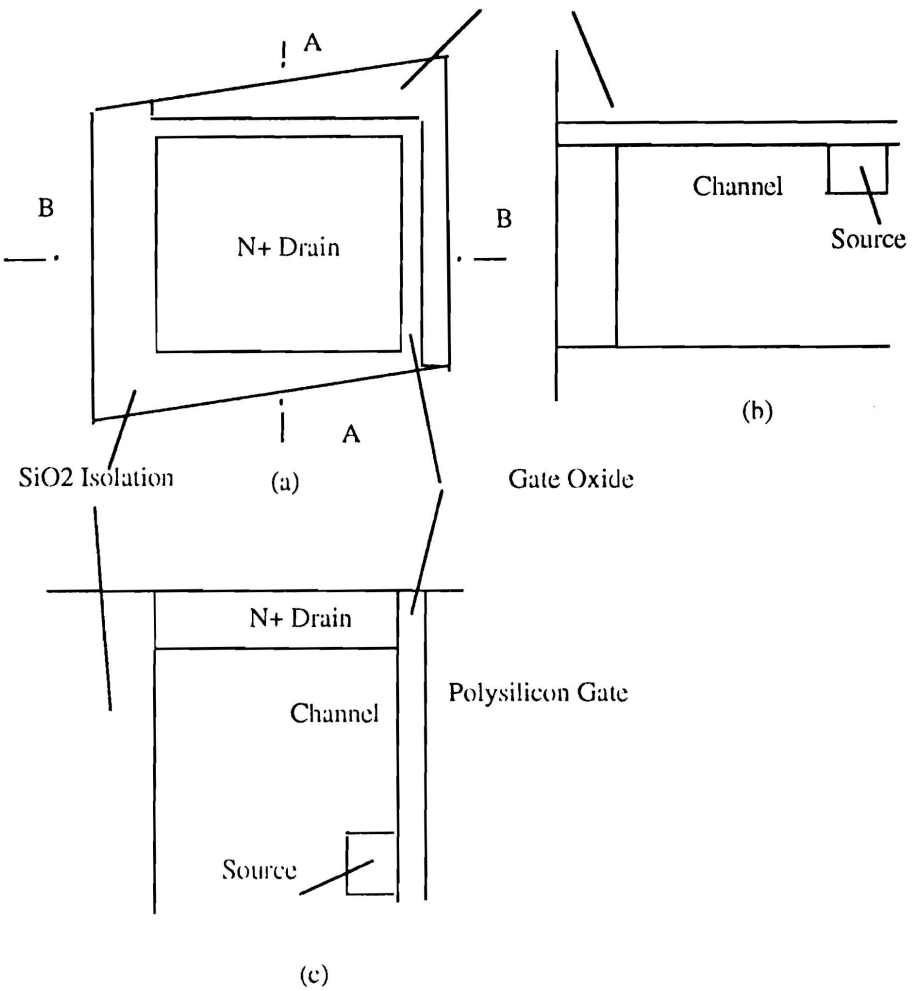

Figure 1. (a) *Top view,* (b) *Cross-Section A-A,* (c) *Cross-Section B-B. The MOS polysilicon gate is formed on two sides of the trench structure.*

1. The MOS polysilicon gate is formed on two sides of the trench structure.
2. The MOS source is formed at the bottom of the trench beneath the polysilicon gate.
3. The drain is the only region formed on the top of the structure to share a minimum planar surface area on the substrate. Therefore more than 70% of the MOS device area could be saved with the proposed structure.

Moreover, due to the vertical nature of the channel in the OVMOS structure, the channel length is independent of the technology linewidth and high performance could be achieved with the OVMOS circuits for any scale of integration.

3. PROPOSED FABRICATION PROCESS STEPS

The proposed fabrication process steps of OVMOS device structure is basically similar to that for 16-MB DRAM [8, 9] and for SGT for Ultra-High-Density LSI's [3]. Figure 2 shows a schematic view and the proposed fabrication process steps for the basic OVMOS for NMOS. First, a p-type well region is formed on the (100) plane of the silicon substrate for threshold voltage adjustment. A doping profile of the p-type well is nearly constant up to a 2 μm depth from the silicon surface. The pillar silicon island, with 1–2 μm height, is formed by a conventional silicon grooving technology. After forming a 25 nm thick gate oxide, $n+$ polysilicon is deposited and etched off, except on a two pillar sidewall and under the mask resist patterns for gate electrode wiring, using the conventional reactive ion etching technique. The two sides surrounding gate structure are also formed by this step. Then, the arsenic ion is implanted to form the source and drain regions. In this case, threshold voltage adjustment is achieved by the well impurity concentration alone. Aluminum metalization is carried out after the contact hole formation.

4. OVMOS DEVICE SIMULATION

The OVMOS transistor has been studied using a two-dimensional device simulator PISCES-IIb [10]. The input device parameters are as follows: Gate oxide thickness = 25 nm, Vertical channel length = 1.5 μm, Substrate doping = 4×10^{15} cm^{-3}, and the threshold voltage is adjusted to be 0.7 V with boron implant dose of 3.2×10^{10} cm^{-2}, which provides a doping concentration of 2×10^{16} cm^{-3} under the gate. Figure 3, shows the transfer characteristics of an OVMOS structure with channel length L = 1.5 μm and substrate bias voltage V_{bb} = 0 and –2.5 volt. The subthreshold slope is 115 and 73 mV/decade respectively. PISCES-IIb is used to compare OVMOS transfer characteristics with those of the conventional planar MOS, using the same channel length and technology parameters. Subthreshold slope of 72 mV/decade is shown for the planar MOS. The simulated output characteristics of OVMOS are shown in Figure 4, for V_g = 1, 3, and 5 V.

A typical simulation of the equipotential contours in OVMOS are shown in Figure 5, for the device with L = 1.5 μm. It is clear that OVMOS provides a long channel behavior, where a constant potential from source to drain in the channel region is shown in the figure and is also due to the correct selection of the doping concentration and operating voltages and consequently the absence of the punch through.

Comparison between the areas occupied by the planar transistor and the proposed OVMOS transistor is shown in Figure 6. The area of OVMOS is about 30% of that of the planar transistor.

5. CONCLUSION

A novel high density OVMOS transistor structure is introduced. More than 70% of the device area can be saved with respect to the planar MOS for the same technology parameter. The proposed fabrication process steps are discussed. PISCES-IIb is used to simulate the output, transfer characteristics, and the equipotential contours in the OVMOS structure.

ACKNOWLEDGEMENTS

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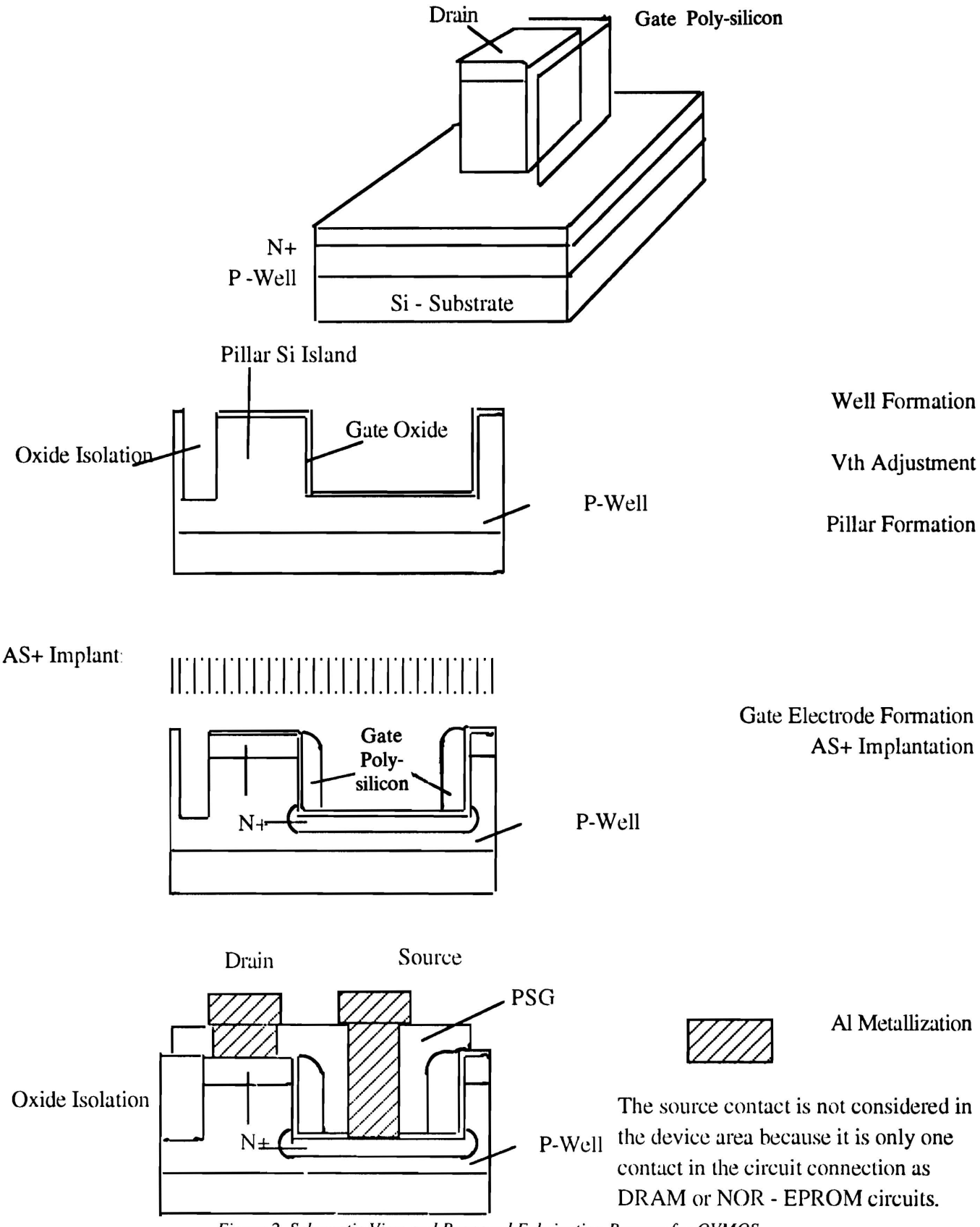

Figure 2. Schematic View and Proposed Fabrication Process for OVMOS.

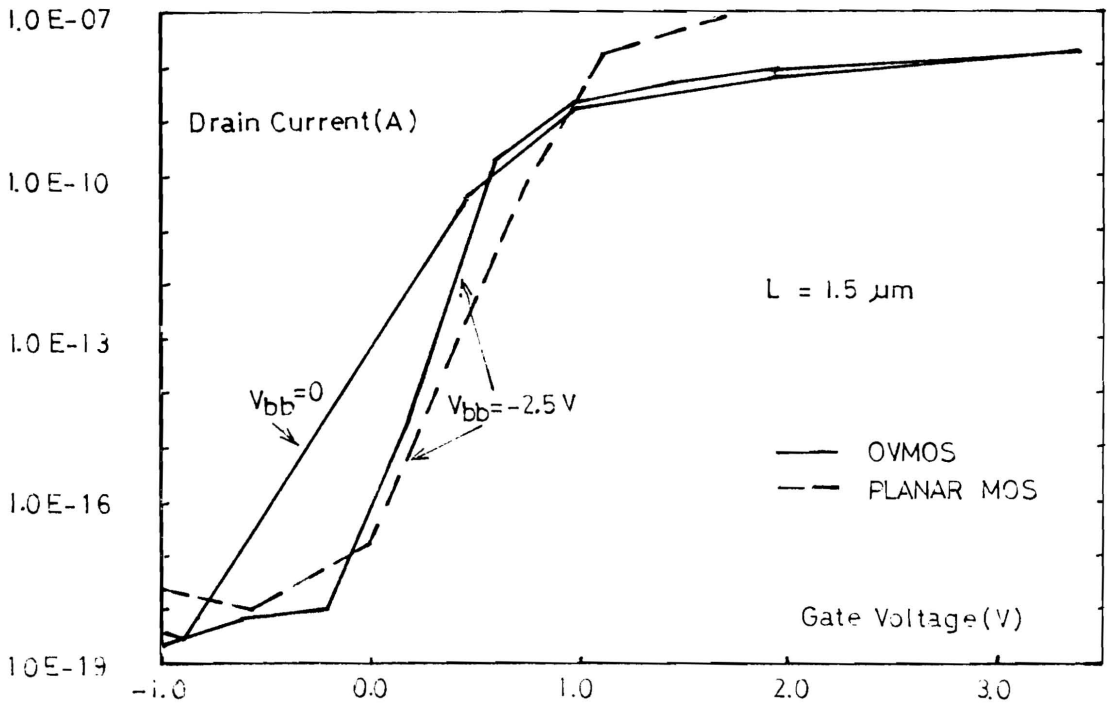

Figure 3. OVMOS Transfer Characteristics.

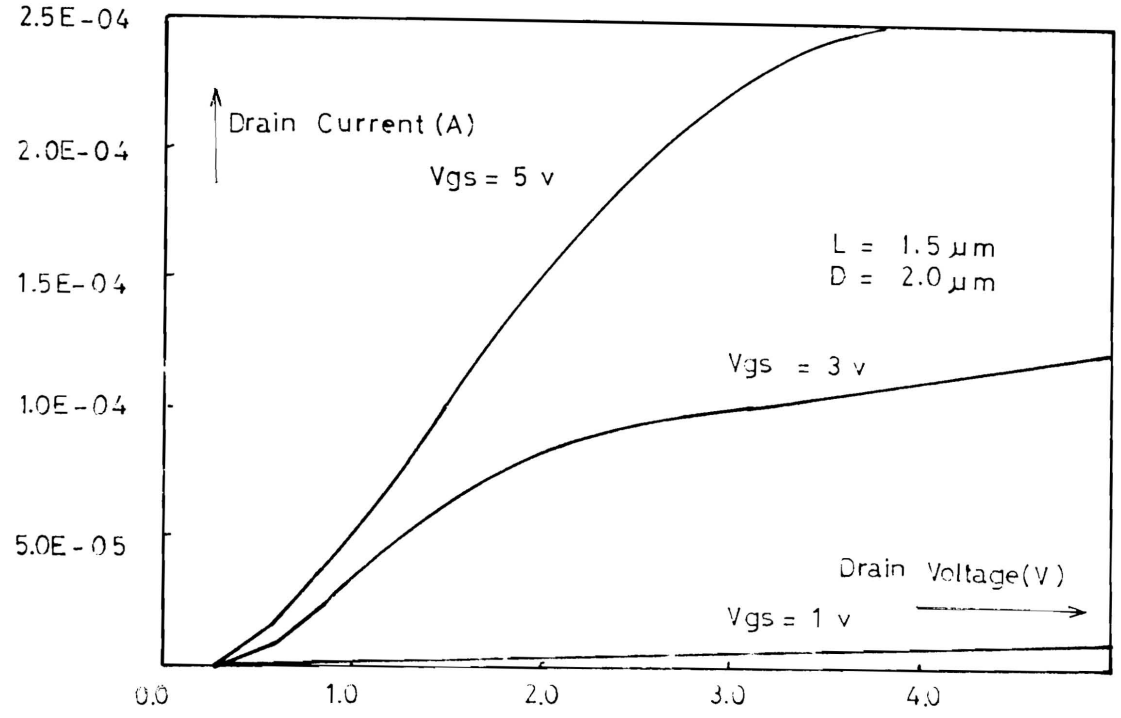

Figure 4. Output Characteristics of OVMOS.

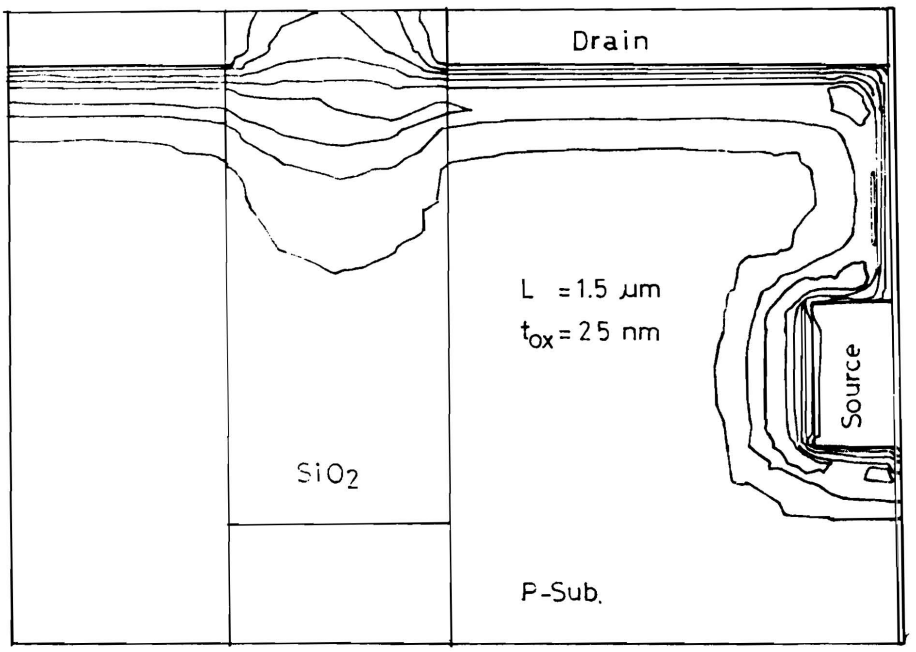

Figure 5. Equipotential Contours in OVMOS.

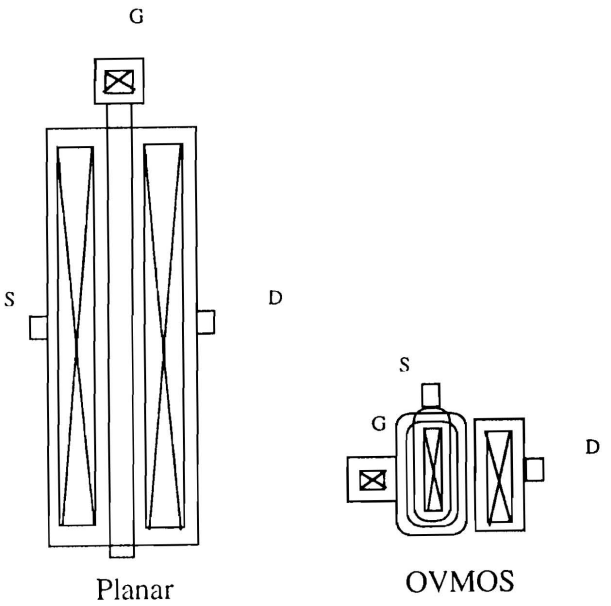

Figure 6. Comparison Between the Area Occupied by the Planar Transistor and the Proposed OVMOS Transistor. The area of OVMOS is about 30% of that for the planar transistor for feature size L = 1.5 μm and device width W = 9 μm.

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