SALICIDE PROCESS FOR SUBMICRON BiCMOS TECHNOLOGY

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الخلاصـة :

نستقصـي في هـذا البحـث ساليسيـد التيتانيـوم المُسْتَحْضَـر على سطـح السيليكون (المشـاب / غير المشاب) عديد البلورات حيث يمكن أن يرافقة تَكَوُّنات غير موغوبٍ فيها مثل : النمو الجانبي للساليسيد على جدار طبقة الأكسيد مما يؤدي إلى وصل المدخل مع المنبع / المصرف، وكذلك تفاعل التيتانيوم مع الأكسيد المجالي مؤدياً إلى وصل الجهاز خلال الدائرة ملغياً عملة. كما قد يحدث اختلاف في صفات الساليسيد حسب نوع وتركيز الشوائب في السيليكون. ولمحاولة فهم ميكانيكية التفاعل قمنا بإجراء عدة تجارب لدراسة معدل نمو الساليسيد، وتفاعل الشوائب والساليسيد، والمعالجة الحرارية السريعة (RTP) لعديد السيليكون - ساليد وتفاعل تايتانيوم / أكسيد، والنمو الجانبي للساليد حسب دالة الحرارة ومجال المعالجة. كما قمنا بتحديد حقائب جهاز ساليسيد BiCMOS بواسطة SEM، ومقاومة التلامس، والمقاومة السطحية، وقياس تسرب تيار الوصلة. بدا لنا أن معالجة الساليسيد المُثلى تناسب الأجهزة الدقيقة جداً ذات أبعادٍ أقلَ من الميكرون .

ABSTRACT

Simultaneous titanium salicide formation on doped/undoped Si and Polysilicon (poly-Si) can be accompanied by undesirable materials effects such as: salicide lateral growth over the sidewall spacer oxide and hence bridging of the gate to source/drain (S/D), Ti reaction with the field oxide, resulting in global shorting of devices and circuits, and variations in salicide properties depending on dopant concentration/type in the Si. To understand the interaction mechanisms, experiments were carried out to study the salicide growth rates, dopant/salicide reactions, rapid thermal processing (RTP) of poly-Si salicidation, Ti/oxide interactions, and salicide lateral growth as a function of temperature and process window. Salicided BiCMOS devices were characterized by SEM, contact resistance, sheet resistance, and junction leakage current measurements. The optimized salicide process exhibited characteristics suitable for submicron devices.

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INTRODUCTION

The self-aligned titanium (Ti) salicide process is used to reduce the sheet resistance (R_s) of the emitter and extrinsic-base areas in bipolar structures, and to reduce the interfacial contact resistance (R_c) to diffusion areas and poly-Si materials in MOS devices [1–8]. The rapid thermal processing (RTP) anneal causes the deposited Ti metal to react with the exposed poly/Si regions, resulting in a low R_sR film. Then a selective wet etch is used to remove the unreacted Ti on the oxide regions. Subsequently, a high-temperature second RTP step is performed to reduce the salicide R_s to its minimum value and to stabilize the film. A simplified MOS device structure is illustrated in Figure 1 where the salicided areas are highlighted. The salicide process interactions with S/D or gate/emitter materials can lead to side effects such as: high R_c due to dopant depletion into the salicide film, incomplete salicide formation, and Ti reaction with the field/side wall spaces (SWS) oxide resulting in conductive Ti oxide global circuit shorting. To avoid these problems, the process parameters require critical optimization. The main issues that directly affect the salicide integration process are dealt with in the present study.

PROCESS, RESULTS, AND DISCUSSION

Salicide Formation

P-type < 100 > Si wafers were used to form silicide films on blanket wafers implanted with As^+ (3×10^{15} cm^{-2} at 70 KeV) or B^+ (2, 2.5, or 3×10^{15} cm^{-2} at 5 KeV). P^+ implanted poly-Si film (1×16 cm^{-2} at 50 KeV) were also used as substrate material. All the implants were activated using A.G. Associates RTP system model 4100 at 1025°C for 40 sec. A 500 Å Ti film was deposited and then reacted with Si using the same RTP system to form salicide material on the As^+, B^+, or undoped single crystal Si or the P^+ poly-Si. The details of the two salicide RTP steps used are discussed below. The optimized salicidation and implantation parameters were implanted in 0.8 μm BiCMOS devices. The RTP system wafer-temperature was determined using the dual pyrometer technique, which depends on the wafer backside emissivity. To ensure accurate RTP temperature measurements for different substrates, the Si backside of all wafers was exposed and cleaned.

First Salicidation RTP Step

The first RTP step is performed at low temperature, enabling the Ti to selectively react with the underlying Si. The temperature of this step is not sufficient to cause complete phase formation of $TiSi_2$. During the first RTP step a thin layer rich with nitrogen (from the annealing ambient) and unreacted Ti is formed at the surface of the salicide film. This layer is subsequently removed by selective wet chemical etching (NH_4OH: H_2O_2: $5H_2O$) for 30 min at room temperature. This wet etch also removes any Ti material located on oxide, but does not attack the salicide material formed on the Si surface, and therefore provides the desired selectivity. The optimum temperature for this RTP step, under the present conditions, was determined to be 700°C/60 sec in N_2. Typical results are shown in Figure 2 where the first RTP step was performed for various materials at $t = 30$ sec). R_s was measured using the Omni Mapping system. The salicide layer exhibited different R_s

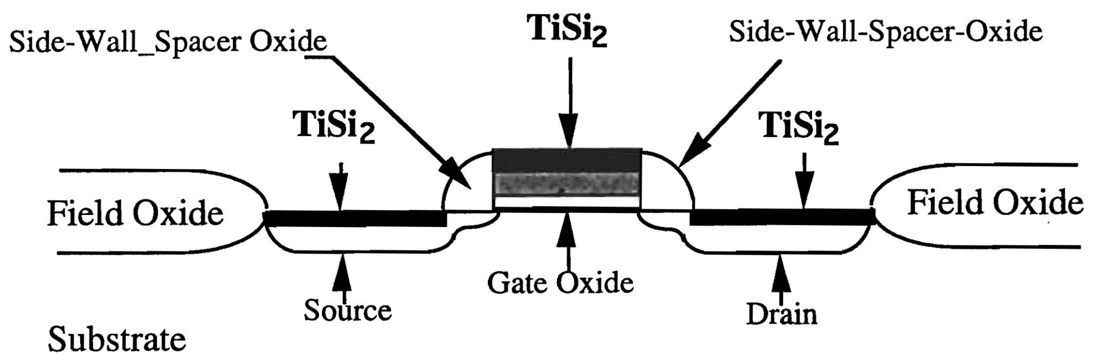

Figure 1. A cross section of a MOSFET showing the salicide film structure, after titanium deposition, first RTP salicidation step, selective wet etching, and the second RTP salicidation step.

values depending on whether the salicide was formed on As^+ or B^+ ($2 \times 10^{15} B^+/cm^2$ doped Si, or P^+ doped poly-Si R_s for the As^+ doped Si at 720°C is 7 Ω/sq, while it is 1.5 Ω/sq for the B^+ material. The observed high R_s in the As^+ diffusion case can be attributed to the retarding effect of the high As^+ dopant concentration on the salicide formation. R_s in the B^+ case is lower than that of films formed on the As^+ material and is comparable to that of films formed on undoped Si.

The first RTP cycle is the most critical RTP step in forming salicide films for submicron geometry devices. The temperature of this step must be kept to a minimum to avoid salicide lateral growth over oxide regions and/or Ti interaction with oxide and consequent global device shorting. Figure 3 shows SEM micrographs for (*a*) properly formed and (*b*) improperly formed salicide films. In case (*a*), an optimized first RTP step temperature of 700°C/60 sec was utilized, resulting in

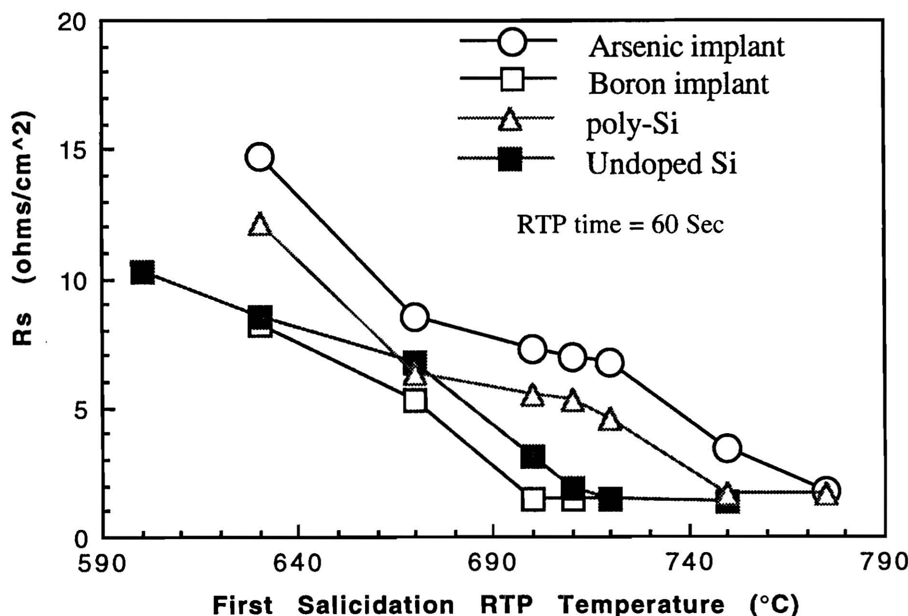

Figure 2(a). Sheet resistance (R_s) versus *first RTP salicidation step temperature* (t = *60 sec), for* As^+ *and* B^+ *diffusions and doped emitter poly-Si and undoped Si substrates.*

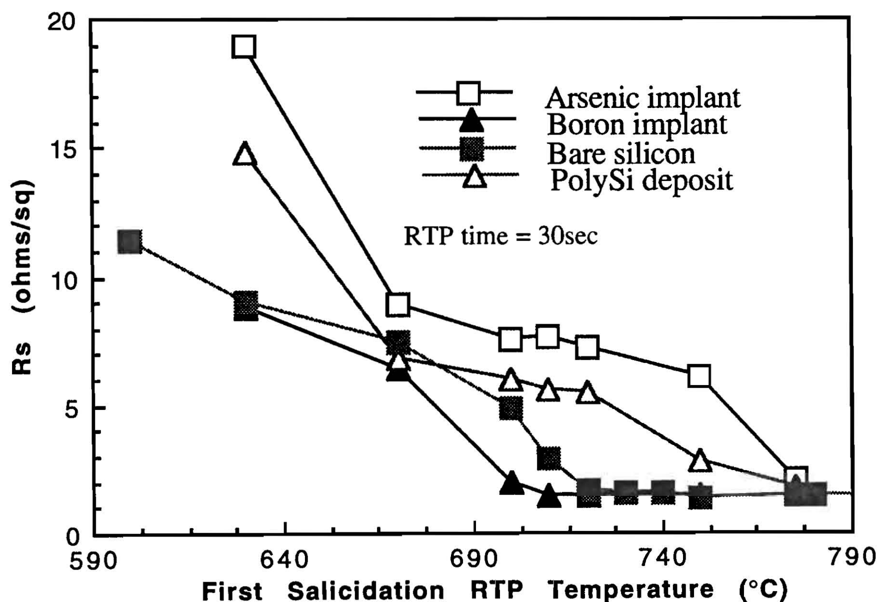

Figure 2(b). Sheet resistance (R_s) versus *first RTP salicidation step temperature* (t = *30 sec), for* As^+ *and* B^+ *diffusions and doped emitter poly-Si and undoped Si substrates.*

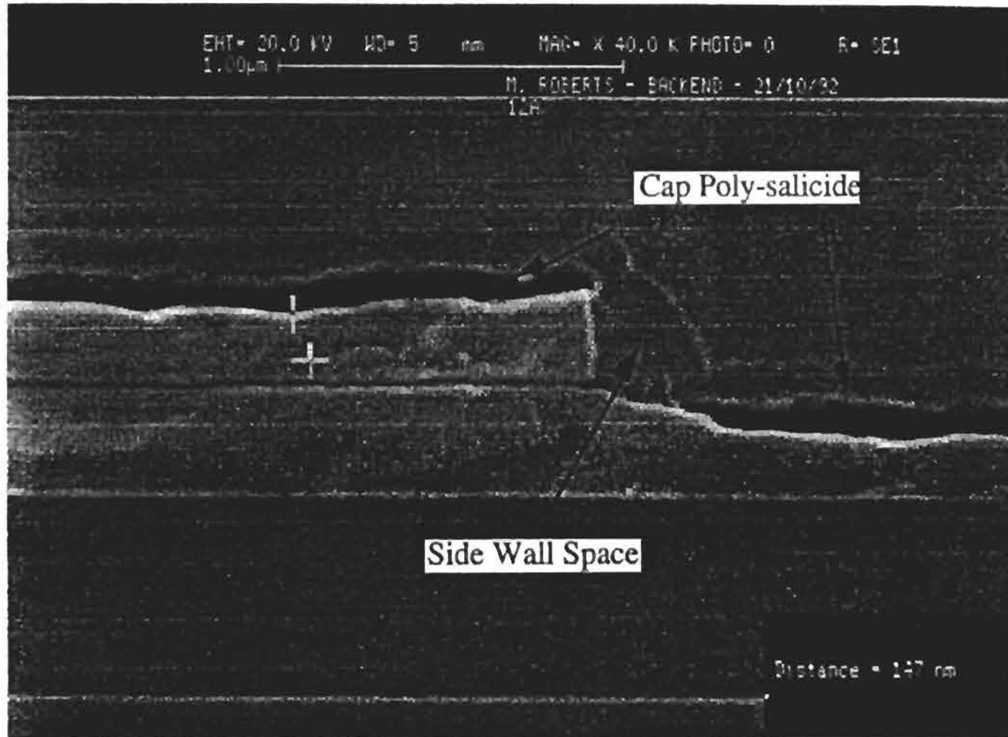

Figure 3(a). SEM micrographs of a properly formed salicide film.

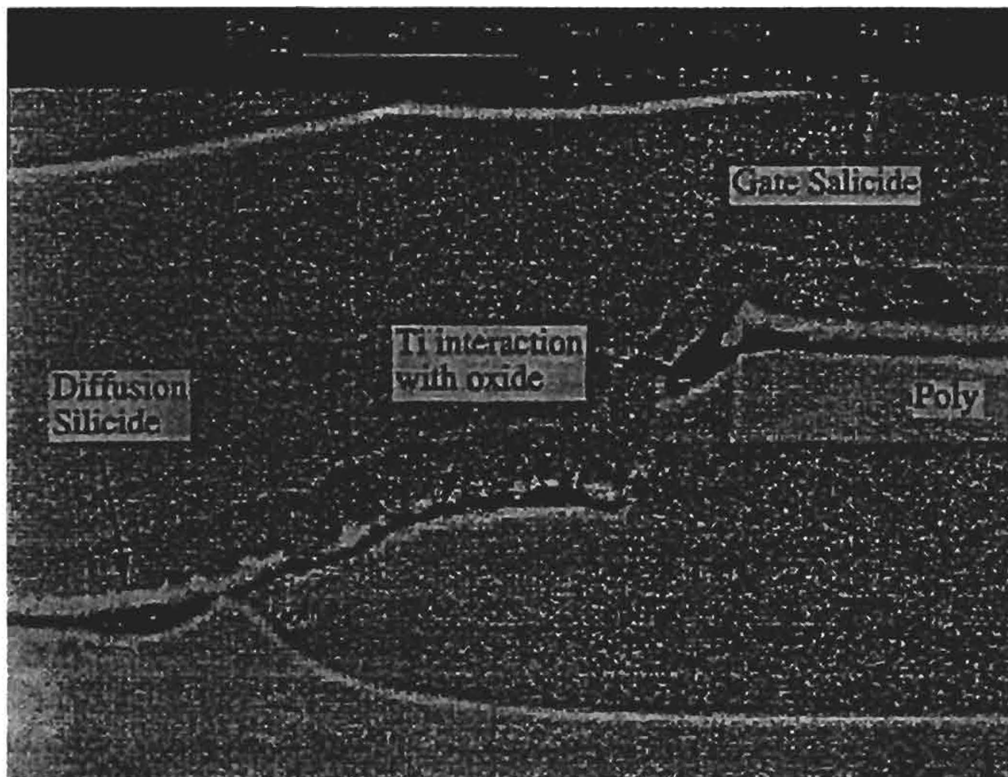

Figure 3(b). SEM micrograph of an improperly formed salicide film.

successful film formation. In case (*b*), the high temperature (750°C) caused the Ti film to react with the field and SWS oxides and thereby form conductive titanium oxide on top of the field oxide, which caused global short circuits. The effect of the RTP time on the salicide properties was only noticeable at low temperature (≤ 700°C) where a 60 sec anneal leads to lower R_s values than the 30 sec cycle. For example, the As^+ + film R_s is 19 Ω/sq and 14 Ω/sq for the 30 sec and the 60 sec anneals (at 630°C), respectively. No Ti interaction with oxides or salicide lateral growth was seen in any case for temperatures ≤ 740°C/60 sec, providing a temperature margin of about 40°C.

Second Salicidation RTP Step

As shown in Figure 4, the R_s ratios between As^+ and B^+ or undoped Si are greater after the wet etch and the second salicidation step than after the first RTP step, because of the removal of the unreacted Ti/TiN film at the surface during the wet etch. In the case of As^+, the amount of Ti/TiN material removed was greater than for the other cases, leading to a thinner final salicide film and hence higher R_s values. The optimum second RTP cycle was determined to be 790°C/sec. The impurity concentration at the salicide-Si interface can decrease by about a factor of two as a result of the salicide RTP process, and therefore the salicide thermal budget must be kept to a minimum in order to avoid too much impurity depletion at the interface which could result in a significant increase in the R_c, as well as salicide–silicon interface current leakage. R_s after the second RTP step (790°C/60 sec) is presented in Figure 4, as a function of the first RTP temperature, for two different RTP times (t = 60 sec and t = 30 sec). In this figure, results are presented for As^+ or B^+ implanted Si as well as for doped emitter Poly-Si and undoped Si substrates.

The RTP time does not have a significant effect on the final results unless the first RTP step was performed at a temperature ≤ 700°C, as can be seen in Figure 4. R_s after the second RTP salicide formation As^+ source/drain diffusion was 2.1Ω/sq and the standard deviation was 3%. The RTP temperature range 790°C ± 15°C was found to have an insignificant effect on device shorts or on the film R_s because this step is performed after the unreacted Ti has been removed and hence there is no question of salicide lateral growth or Ti reaction with oxides at this point. Temperatures beyond the 790°C range, however, may result in Ti diffusion into the junction region and therefore result in excessive junction leakage current. On the other hand, lower temperatures will lead to unstable films with high R_s especially for As^+ diffusions and poly-Si materials. Therefore, the optimized operating conditions must be reached to ensure a stable process. Table 1 shows typical device results for a 0.8 μm BiCMOS process using the optimized process. The uniformity and reproductivity of these results were within the 95% range.

Thermal Budget Optimization

Salicidation of As^+ and B^+ diffusion areas, gate poly, and emitter poly areas requires different thermal budgets due to differences in materials properties and doping levels. For example, As^+ diffusions require a higher temperature to form proper salicide than do B^+ diffusions, because heavy As^+ doping impedes salicide formation and therefore results in too thin a salicide film. Increasing the temperature to overcome this problem could lead to too thick a salicide layer in the B^+ region and consequently too much Si consumption. An initial Ti film of 500 Å was determined to be the optimum thickness to limit the Si consumption in the B^+ region. High temperatures can lead to R_c problems, as a result of dopant migration from the Si

Table 1. Typical Results for the $TiSi_2$ Film Sheet, Resistance R_s (Ω/Sq), $TiSi_2$/Si Contact Resistance R_{c1} (Ω/Link), and the $TiSi_2$/Metal Contact Resistance R_{c2} (Ω/Link) as Extracted From Contact Chains (Total of 2500 Contacts) With 0.8 μm Contact Hole Size. Each link is comprised of two contacts and one square (1.8 μm × 1.8 μm) in between.

	R_s	R_{c1}	R_{c2}
N^+ Source/Drain	3.40	140.0	14.0
P^+ Source/Drain	2.5	255.0	9.5
N^+ Gate Poly	3.5	–	16
N^+ Emitter Poly	4.55	–	12

into the salicide film. Therefore, all the trade-offs must be balanced to satisfy the thermal budget requirements for all doped regions and materials. The implant thermal activation cycle must also be optimized to obtain adequate impurity concentration at the surface, since too much dopant at the surface would impede salicide growth. On the other hand, too little dopant would result in a leaky Schottky contact instead of an ohmic contact at the Si/salicide interface. The activation cycle results in impurity diffusion deeper into the bulk, thus less dopant remains at the surface where the Ti reaction with Si takes place. For inactivated high dose implants ($1 \times 10^{16} As^{+}/cm^{2}$), the reaction between the Ti and Si is impeded, even at high salicidation

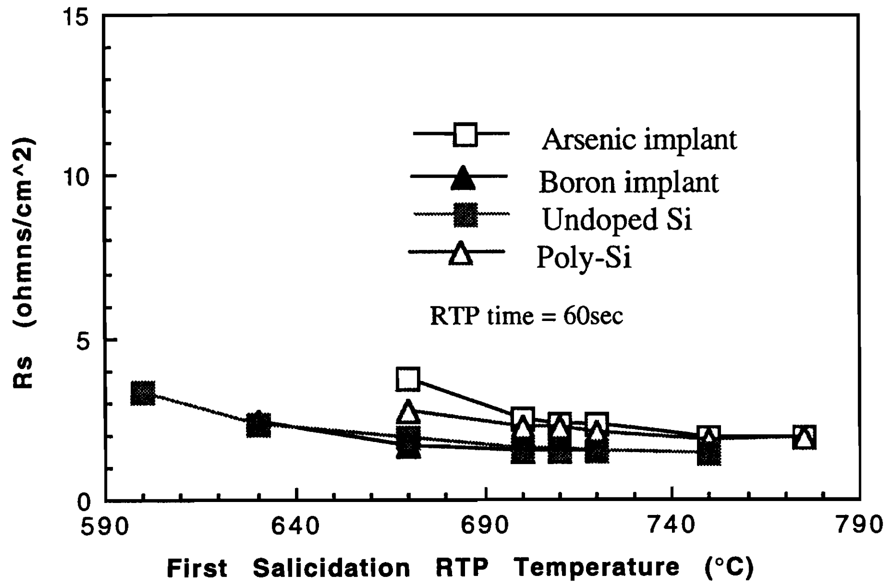

Figure 4(a). Sheet resistance (R_s) versus first RTP salicidation step temperature (t = 60 sec), after the unreacted Ti etch and the second RTP salicidation step (t = 60 sec) have been performed, for As^+ and B^+ diffusions and doped emitter poly-Si and undoped single Si substrates.

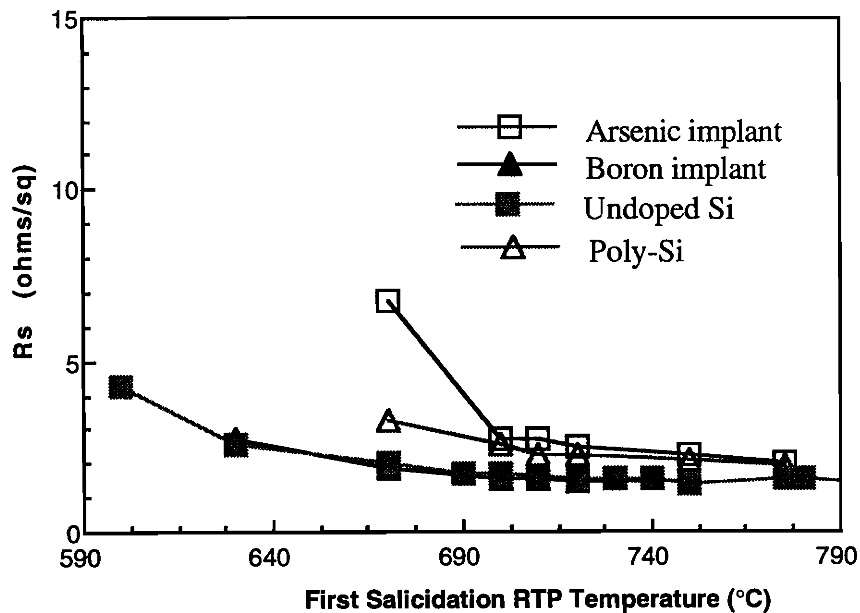

Figure 4(b). Sheet resistance (R_s) versus first RTP salicidation step temperature (t = 30 sec), after the unreacted Ti etch and the second RTP salicidation step (t = 60 sec) have been performed, for As^+ and B^+ diffusions and doped emitter poly-Si and undoped single crystal Si substrates.

temperatures [9]. The effect of the activation cycle on the final device R_c is demonstrated in Figure 5 for 0.8 μm devices. The implantation dose is a major factor in determining the effect of the activation cycle on the salicide process; for an implant dose less than 3×10^{15} cm^{-2} the activation cycle has no significant effect on the RTP salicidation temperature, but will have a significant effect on R_c, as illustrated in Figure 5.

Si Consumption/Dopant Depletion

For shallow junctions, as in the present study (0.25 μm), the amount of Si required to selectively react with the Ti to form salicide without Ti penetration into the junction depletion region is one of the critical limitations of the salicide process. Thus, the implantation conditions and the activation thermal cycle were designed in such a way to maintain a buffer zone between the salicide/Si interface and the bottom of the junction in order to avoid excessive junction leakage current. 1000 Å of Si is consumed by the 500 Å of Ti to form a salicide film of 1000 Å. This leaves a buffer zone of about 0.15 μm. The junction leakage current depends strongly on the width of this buffer zone.

During the salicide process formation, the dopants segregate from the diffused regions to the $TiSi_2$ layer and then diffuse through the salicide film to the external annealing ambient. The large dopant diffusivity in titanium salicide [10, 11] increases this effort and hence can result in a significant increase in R_c. Four parameters control the R_c values: the starting implantation conditions, salicidation temperatures, dopant activation temperature, and the salicide final thickness. These parameters were optimized in order to achieve R_c values compatible with submicron device performance, especially for the B^+ diffusion R_c which normally suffers the most. A thicker Ti film increases the amount of dopant depleted from the Si junction regions [9]. A Ti film of 800 Å resulted in 80% loss of the total implanted dose, compared to 60% dopant loss in the case of the 500 Å Ti film. Therefore, the film thickness must be taken into account in designing the implantation and salicidation processing conditions.

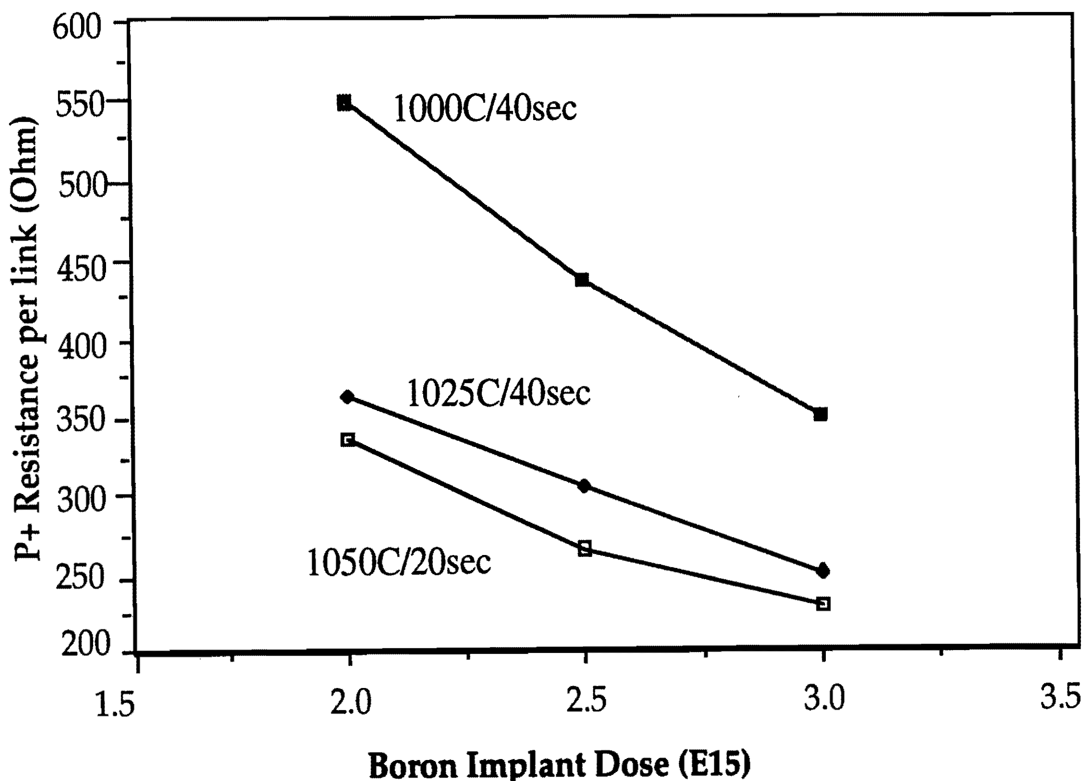

Figure 5. The B^+ contact resistance per link as a function of the RTP activation thermal cycle and the boron implant dose.

Salicide/Si Interface Resistance (R_c)

The effects of the salicide film, B^+ implantation dose, and the junction activation cycle on the interface R_c were studied. The three B^+ doses used were: 2×10^{15}, 2.5×10^{15}, and 3×10^{15} B^+/cm^2 at 5 KeV. The doping concentration level at the salicide/Si interface is affected by the implant activation cycle which consequently will affect the salicide properties. Figure 5 shows R_c as a function of the B^+ dose and the activation thermal cycle. R_c dropped sharply to 61% of its value as the activation cycle was increased from 1000°C to 1025°C. This improvement in R_c is due to a higher impurity concentration at the salicide/Si interface when the 1025°C cycle is used, as compared to the 1000°C cycle case. As observed from Figure 5, there is a linear dependency of R_c on the B^+ dose; R_c dropped by an additional 70% as the dose was increased from 2×10^{15} to 3×10^{15} cm^{-2}, in the case of the 1025°C activation cycle. The optimum activation and implantation parameters that gave the lowest R_c values, without causing any deleterious short channel effects, were 1025°C/40 sec, and 3×10^{15} B^+/cm^2 at 5 KeV, respectively.

The interfacial resistance (R_c) between the salicide film and the underlying silicon, for 0.8 μm contact holes, was measured (in ohms) using a Kelvin structure. The effect of the first RTP step temperature and the initial titanium film thickness on that resistance was also evaluated. As can be seen in Figure 6, R_c for N^+ areas does not change significantly as a result of changing the Ti thickness from 500 Å to 400 Å or varying the first RTP temperature in the range 690°C ± 15°C. This is because the final salicide thickness in the N^+ case is mainly controlled by the As^+ doping level. However, in the case of B^+ R_c increased as the first RTP temperature increased and dropped when the Ti thickness was dropped from 500 Å to 400 Å. This drop in the B^+ R_c in the case of thinner salicide is because the $TiSi_2$/Si interface is located at a higher B^+ doping concentration.

Junction Leakage Current

To investigate the salicided junction leakage current variation with salicide parameters (thickness and RTP cycle), shallow $N^+/P^+/N$ junctions of 0.3 or 0.25 μm deep, respectively, were fabricated using the optimized implant, RTP cycles, and salicide parameters described above. The N^+ junctions were implanted with arsenic ($3.5 \times 10^{15}/cm^2$, 70 KeV) and the P^+ junctions were implanted with boron ($3 \times 10^{15}/cm^2$, 5 KeV). After junction RTP activation at 1025°C/40 sec the salicide was formed using the two RTP step approach as described earlier. Two titanium thickness (400 Å and 500 Å) and various first salicide RTP step cycles were used. Then, 0.8 μm contact holes were formed and a TiN layer was deposited to act as a diffusion barrier and as an adhesion layer to tungsten interconnects. The contact holes were also filled with tungsten during the interconnect formation. The final junction/salicide/contact/interconnect structure is illustrated in Figure 7. Current–voltage measurements were performed on a large number of devices with various geometries. The measured junction leakage current is illustrated in Figures 8 and 9 for edge intensive N^+ and P^+ junctions, respectively. The leakage current density is about or below 15 nA/cm^2 at 5 V reverse bias for both N^+ and P^+ junctions. The area intensive leakage current density was below 10 nA/cm^2 (Figure 10). The thermal stability and integrity of the junction contact structure was also examined at 100°C, no excessive leakage current was detected nor abnormal electromigration behavior was observed.

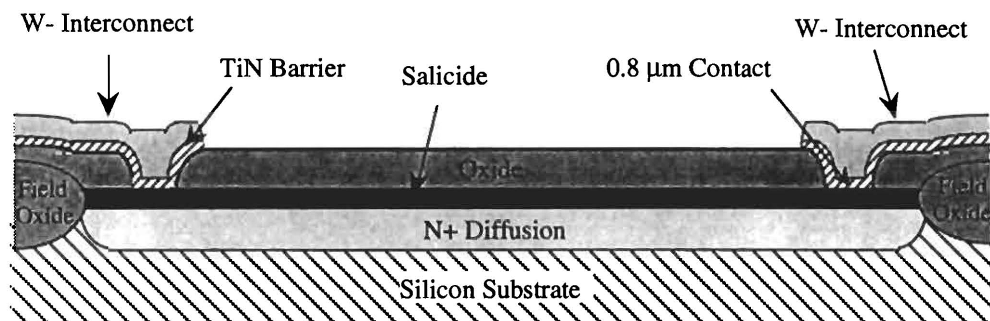

Figure 6. The final contact structure showing the salicide film in the diffusion region and the tungsten interconnect. A similar structure was used to measure the contact resistances and the junction leakage currents.

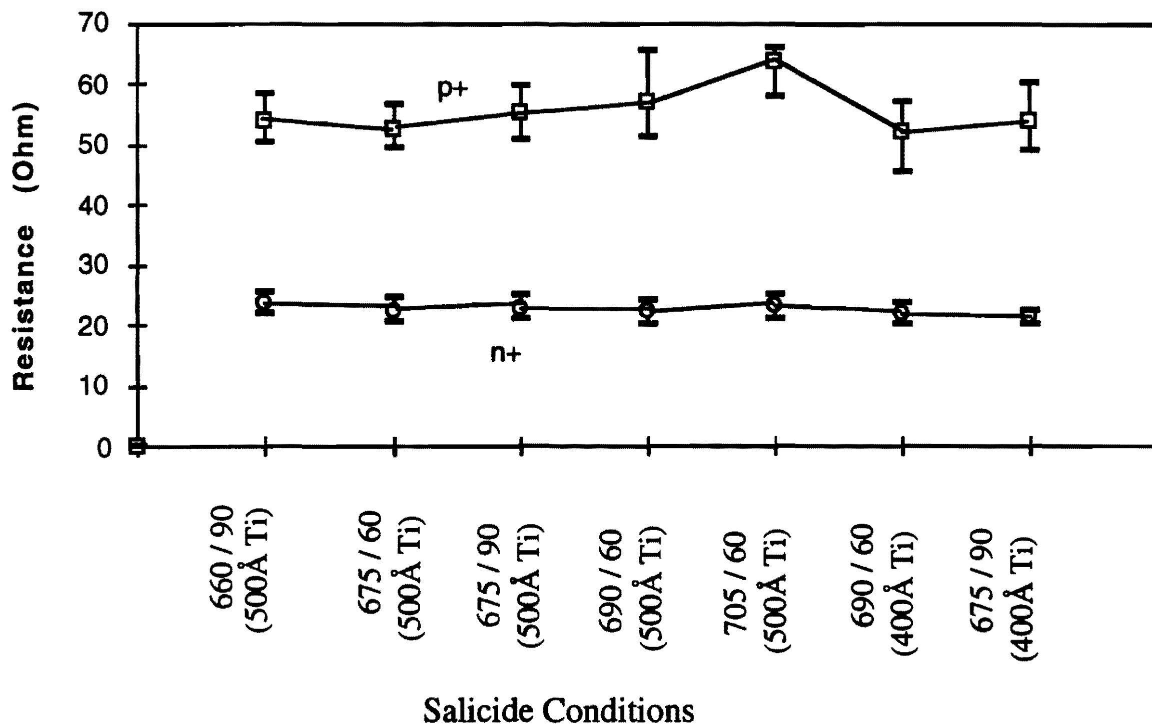

Figure 7. Salicide first RTP anneal step and titanium film thickness effect on contact resistance of salicide to N^+/P or P^+/N Si junctions measured using kelvin structure.

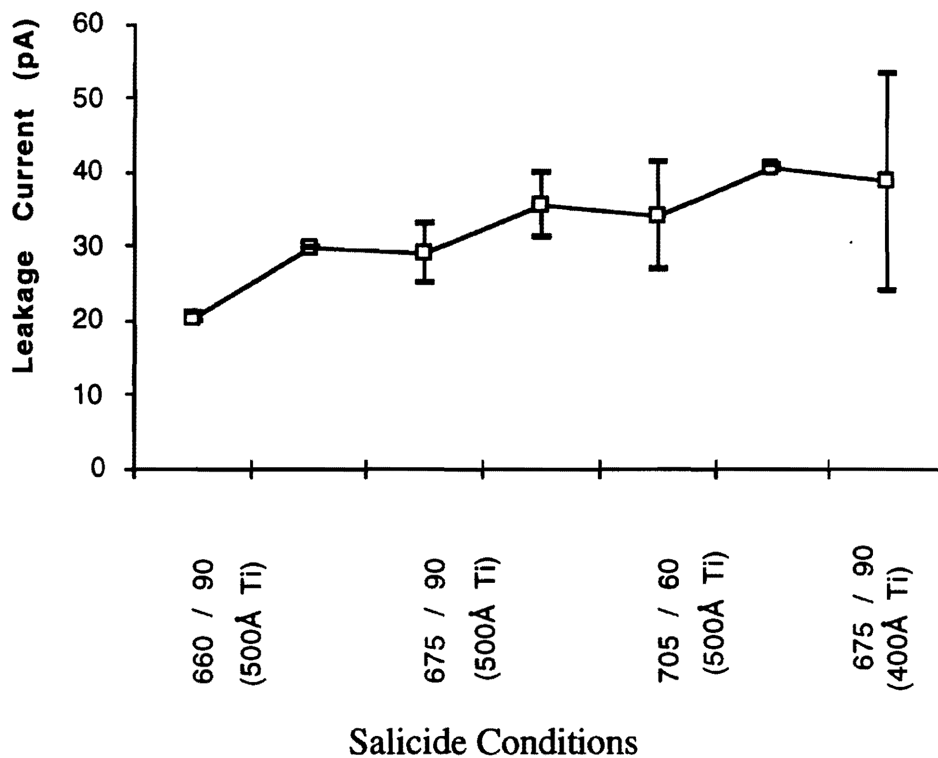

Figure 8. The effect of the first salicide RTP anneal step and the titanium thickness on the leakage current of edge intensive N^+/P diodes.

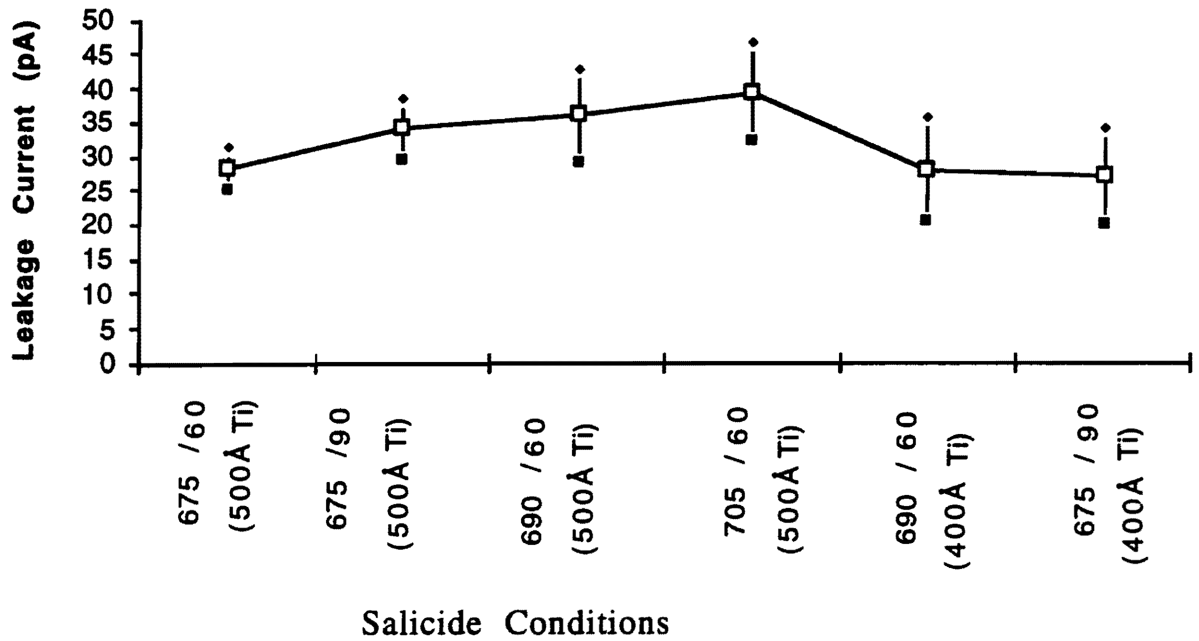

Figure 9. The effect of salicide first RTP anneal step (temperature/time) and titanium thickness on the leakage current of area intensive P^+/N diodes.

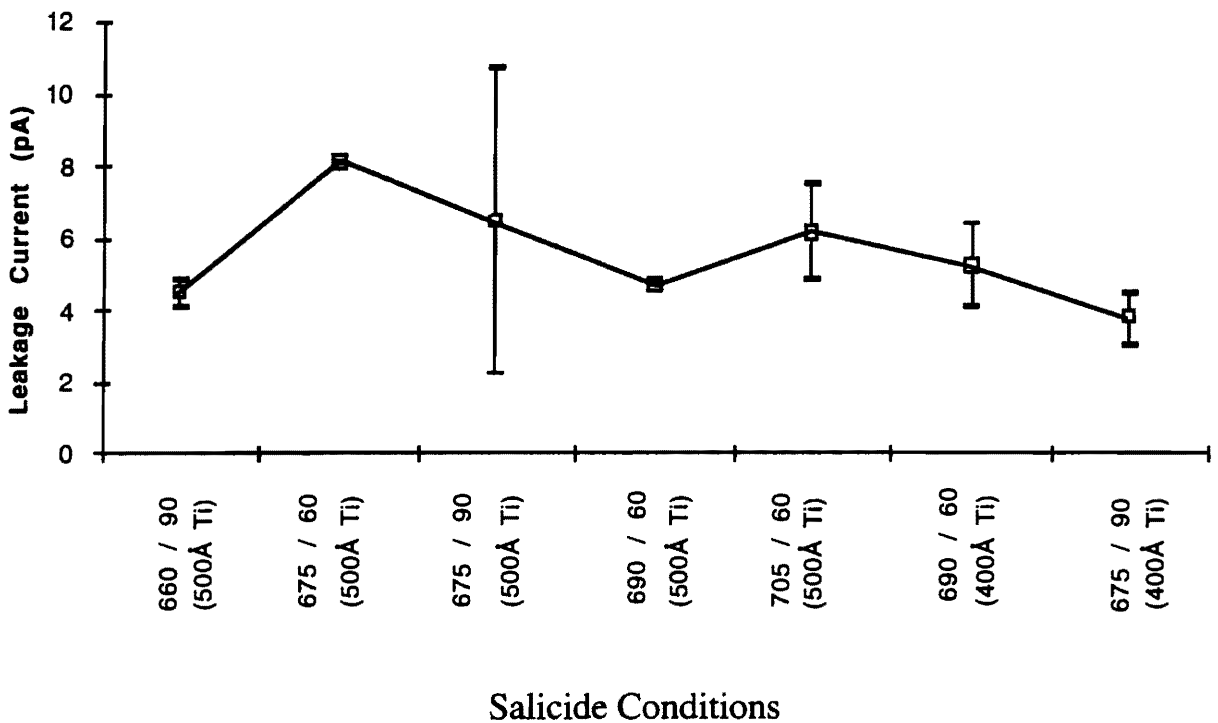

Figure 10. The effect of salicide first RTP anneal step (temperature/time) and titanium thickness on the leakage current of area intensive N^+/P diodes.

CONCLUSIONS

A self aligned titanium salicide process for 0.8 μm BiCMOS technology has been developed, optimized, and analyzed. The process interactions has been taken into account in optimizing the RTP thermal budget, titanium film thickness, and implantation conditions. The contact resistance to P^+ junctions was higher than that for N^+ junctions because of the lower doping level in the former case. The final salicide film sheet resistances for diffusion and polysilicon areas were suitable for high performance 0.8 μm devices. The total leakage currents for salicide junctions were below 25×10^{-9} A/cm^2, which is considered low for the present type of structure.

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