ON THE STICKING PROBABILITY OF CESIUM ON SILICON(111) SURFACES

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الخلاصة :

ان معامل التصاق السيزيوم على سطوح السلكون لا يتجاوز ٠,٢ على درجات الحرارة العادية وعلى درجة حرارة المختبر لا يمكن تغطية السلكون بطبقة كاملة من مادة السيزيوم ، ولكن على درجة حرارة سائل النيتروجين يمكن تغطية السلكون بطبقات متعددة من السيزيوم .

ABSTRACT

The sticking probablity of cesium on Si(111) surfaces is found to be about 0.2 at room temperature. Multilayers of cesium on silicon can only be formed on cold substrates. At room temperature only submonolayers of cesium are bound strongly enough to the surface.

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INTRODUCTION

One of the most useful instrumental techniques in characterizing solid surfaces is photo-electric emission, i.e. the emission of electrons caused by the irradiation of matter by photons. In this technique one shines light onto a sample and studies the properties of the emitted electrons. The emission of electrons in such an experiment is thought to occur in three steps:

1. the excitation of an electron by absorption of a photon;
2. the transport of the electron to the surface;
3. the escape of the electron through the surface.

Semiconductors are known to be the most efficient photo-electron emitters because they have smaller reflectivity and weaker electron–electron interaction than metals, while having lower threshold energies than insulators.

An obvious prerequisite for photo-electron emission to be useful is that a large fraction of the excited electrons be emitted. In other words, the energy barrier at the surface must be lower than most final energies. This can be achieved by the adsorption of small amounts of a suitable substance like, for instance, cesium. In practice, the amounts adsorbed are less than one monolayer.

Cesium deposition on semiconductors lowers the work function of the underlying substrate. This reduction in the work function is accompanied by an increase in photo-electric yield and a decrease in the threshold energies (extension to longer wavelength light). So cesium deposition produces more practical photocathodes.

These facts make the effect of cesium adsorption on the electronic properties of semiconductor surfaces and the mechanism involved in the interaction between the adsorbed cesium and the surface of great interest from both theoretical and practical points of view.

In this paper we will comment on the sticking probability of cesium on Si(111) surfaces and will present experimental evidence to show a strong dependence of this probability on the temperature of the underlying substrate.

THE STICKING PROBABILITY OF CESIUM ON Si(111) SURFACES

Cesium is usually deposited on a surface by one of the two methods:

1. Atomic cesium is produced by passing a current through a small boat (called SAES getter dispenser) enriched with cesium metal. In this case relative coverages are estimated by measuring the times of deposition.
2. Ionic cesium is obtained by passing a current through a platinum ribbon covered with cesium zeolite, and biasing the substrate with a small negative voltage. Here, coverages are calculated by measuring the cesium ion current arriving at the substrate from the zeolite source and using the formula [1]:

$$n = \frac{1}{eA} \int_0^t I(t)\, \mathrm{d}t$$

where I is the cesium ion current, A is the area of the substrate, e is the electronic charge, t is the time and n is the number of cesium ions per unit area.

This formula is approximate because it is not guaranteed that all cesium leaving the source is ionized; also it is not necessary that all detected cesium (by current measurement) stays on the surface.

Many researchers assume a high sticking coefficient of alkali metals on semiconductor surfaces. Allen and Gobeli [2] reported that the sticking coefficient of cesium on silicon and germanium surfaces is high at low coverage and drops to nearly zero as the monolayer condition is approached. The sticking coefficient of cesium on p^+-InP surfaces was assumed to be unity by Bell and Uebbing [3]. Mönch [4], studying cesium on silicon surfaces, reported that the sticking probability is always unity. Chen [5] generalized this assumption to Na on GaAs surfaces and assumed that the sticking coefficient is unity in this case. The sticking coefficient of Cs on GaAs(110) surfaces was also assumed to be unity [6]. Our findings on cesiated Si(111) surfaces cast a serious doubt on these assumptions.

During the course of our experimental work, we

deposited cesium with the silicon substrate kept at room temperature in one case and cooled to 100°K in the other. In the following we present the results on (1Ω cm *n*-type) silicon with surfaces prepared by cleavage in ultrahigh vacuum to expose (111) planes. An SAES getter dispenser was used as the cesium source. Cesiated surfaces were characterized by means of LEED, Auger, as well as photo-electron emission studies. Relative amounts of cesium are reported in our studies due to the lack of the precise knowledge of the sticking probability.

Figure 1 shows the results of such studies when the surface was cesiated at room temperature, while Figure 2 shows the results when the same surface was cesiated at 100°K. In these figures we show the energy distribution curves (EDC) measured at $h\nu = 6.25$ eV, and the Auger spectra (AES) measured at $V_P = 400$ eV (the primary energy of the incident electrons). These measurements were performed on the clean surface and also on the surface after successive cesiation. All measurements were performed in a stainless steel chamber at base pressure of 2×10^{-10} Torr.

RESULTS FROM Si(111) SURFACES CESIATED AT ROOM TEMPERATURE

In Figure 1, row (A) characterizes the clean surface, and shows the high energy end from Ta metal to establish the Fermi level. The clean surfaces exhibited a (7 × 7) LEED pattern. One also notices the silicon Auger peak at 91 eV. The work function of the clean surface was found to be 4.70 eV.

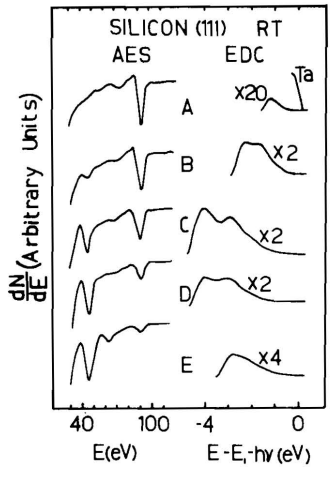

Figure 1. Auger Spectra (AES) and Energy Distributions (EDC) from Si(111) Surface Cesiated at Room Temperature

The curves in row (B) were measured after exposing the surface to the cesium source for 10 s. The work function dropped to 3.45 eV while the LEED pattern remained the same, (7 × 7). Traces of cesium were noticed in the (AES) curve at $E = 47$ eV.

Depositing more cesium, making the total time of exposure 30 s, produced the curves in row (C). The work function decreased to 1.60 eV, and the LEED displayed faint (7 × 7) spots with a good (1 × 1) pattern. The Auger peak of silicon decreased and that of cesium increased.

The curves in group (D) were measured when the total time of cesium deposition was 90 s. The work function was found to be 1.70 eV, and the LEED pattern showed a good (1 × 1) pattern. The Auger peaks showed more decrease in silicon and increase in cesium.

More cesium was deposited on the surface, making the total time of exposure 390 s, till the LEED pattern disappeared. Then the last group of curves, (E), was measured. It is interesting to note that the work function increased at this cesium coverage. The Auger curve, however, still shows some silicon.

Increasing the time of cesium deposition on the surface did not result in any changes in the features noticed in curves (E). The silicon Auger peak was always noticeable. Saturation of coverage was already achieved [7].

RESULTS FROM Si(111) SURFACES CESIATED AT 100°K

Figure 2, on the other hand, shows the results from the same surface of the same silicon crystal. The crystal was first cooled down to 100°K then cesiated.

Curves (A) characterize the clean surface as before, where the LEED displayed a (7 × 7) pattern.

Curves (B) summarize the results of the measurements after the cold surface was exposed to the cesium source for only 2 s. After this short time of exposure the work function decreased to 3.53 eV and the LEED showed a faint (7 × 7) with a (1 × 1) pattern. The cesium Auger peak was also noticeable.

Curves (C) were measured after a total time of 10 s of cesium exposure. The work function was found to be 2.25 eV and the LEED displayed a (1 × 1) pattern. It is interesting to note that the silicon Auger peak decreased drastically at this cesium coverage while the cesium peak increased.

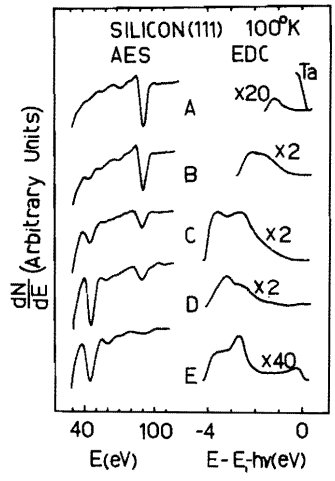

Figure 2. Auger Spectra (AES) and Energy Distributions (EDC) from Si(111) Surface Cesiated at 100°K

The LEED pattern disappeared when the total time of exposure to cesium was 20 s. At that coverage we measured curves (D). The work function remained the same (2.25 eV) as in curves (C). The silicon Auger peak decreased further, and that of cesium increased.

The last set of these curves, (E), was measured after the surface was exposed to the cesium beam for a total time of 60 s. At this coverage no LEED pattern was noticed, as expected, and the silicon Auger peak disappeared totally. The work function was 2.20 eV. The (EDC) showed metallic character at the Fermi level. This indicates that the silicon surface was covered with a thick layer of cesium.

It was noticed also that the measured properties of the surface cesiated at room temperature were reversible functions of temperture. In other words, cooling the surface used in the measurements of curves (E), Figure 1, to 100°K and warming it up again to room temperature restored the same features obtained before.

The properties of the surfaces cesiated at 100°K were irreversible functions of temperature; the features obtained in curves (E), Figure 2, were not restored when the sample was warmed up to room temperature and cooled down.

These observations indicate that multilayers of cesium were only formed on cold substrates. At room temperature, only a submonolayer of cesium is bound strongly enough to remain on the surface and affect the surface properties of silicon.

One concludes that the sticking probability of cesium on semiconductor surfaces is a function of temperature. If this probability is assumed to be unity at 100°K, then by comparing curves D in Figures 1 and 2 one estimates the sticking probability of cesium on Si(111) surface to be about 0.2 at room temperature.

CONCLUSIONS

LEED, Auger and photo-electron emission measurements on cesiated silicon surfaces showed that it is impossible to cover these surfaces with multilayers of cesium at room temperature. The sticking probabilty of cesium on silicon surfaces is found to be around 0.2 at room temperature. The properties of silicon surfaces cesiated at room temperature are reversible functions of temperature, i.e. cooling the surface below room temperature and heating it up to room temperature restores the observed properties. On the other hand, the observed properties of cold cesiated surfaces are irreversible functions of temperature, i.e. warming the cold cesiated surface to room temperature and cooling it back to 100°K does not restore the observed properties.

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