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A Fast Self Adjusting PLD-based Three-phase Firing Circuit for Phase Angle Control Applications

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Abstract. The paper presents a fast, simple and configurable scheme to automatically provide the correct firing pulses for the working thyristors irrespective of any mistake that might happen during connections, in the application of four-wire three-phase AC voltage controller system. The proposed scheme can readjust itself in case of a missed connection or sequence alteration and it is built around a single chip programmable logic device with self generated firing pulses and capable of readjusting the firing circuit against any phase or sequence alteration in 8.4 seconds. The system has additional advantages like the ability of detecting the faulty thyristors, if any, and built in self test routine. Experimental results verify the principle of operation.

I. Introduction

Thyristors are widely used for the control of power in both AC and DC systems. This is due to their advantages, such as relatively small size, low losses and relatively fast switching. Apart from many uses, such an AC voltage controller, which is used to control the three-phase AC power in control of induction heating, light, reactive power and speed of AC motors (Alolah *et al.*, 1990; Abou-Elela *et al.*, 1994). The phase angle control is a well established technique and commonly applied in these applications. A number of different three-phase circuit configurations can be used to achieve the required voltage control (Abou-Elela *et al.*, 1994). Each configuration employs six thyristors or three triacs, connected between the supply and the load. However, only those configurations in which each phase operates independently of the other two phases give balanced and symmetrical output voltages. These configurations may be classified as branch-controlled, line-controlled and neutral point-controlled configuration (Abou-Elela *et al.*, 1994).

The essential part of the phase angle control system is the firing circuit. A good general-purpose three-phase firing circuit should conform several common requirements (Alolah *et al.*, 1990). One of the most important of them is the self adjustment against any phase and/or sequence alterations. Consequently, if this requirement is not satisfied, a manual adjustment must be adapted during their use.

A scheme to meet self adjusting correction circuit has been proposed (Abou-Elela *et al.*, 1994; Abou-Elela *et al.*, 1998). The system automatically provides the correct firing pulses for the working thyristors, irrespective of any mistake introduced during connecting the firing circuit. It starts its operation with the power switching ON/OFF or just after any phase and/or sequence alterations. The circuit stops at the state of correct firing of all the working thyristors of the AC controller and then remains in a stand-by mode.

To reach the instant of correct firing, the average value of the neutral current is detected using a comparator circuit whose output is used to stop the scanning process. The principle of operation depends on scanning all possible connections between the six firing signals and the thyristors, as shown in functional block diagram in Fig. 1. The scheme consists of a scanning circuit, indicating circuit and control logic, implemented using off-the-shelf conventional discrete digital and analog components and consumes about 28.8 seconds to capture the correct firing sequence. The scanning circuit is the

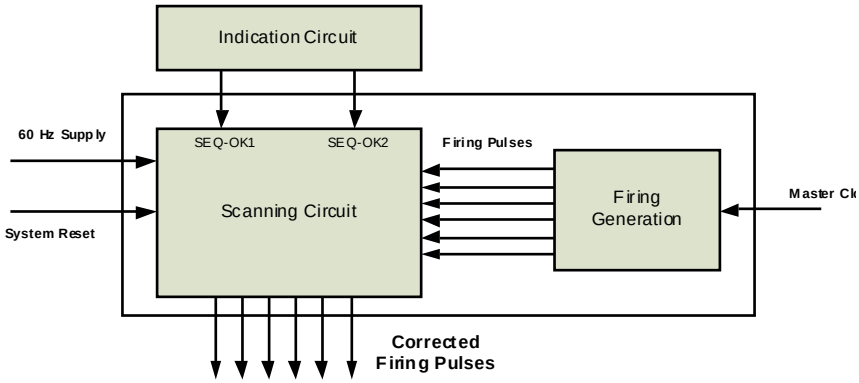

Fig. 1. Simplified functional block diagram for the scanning system.

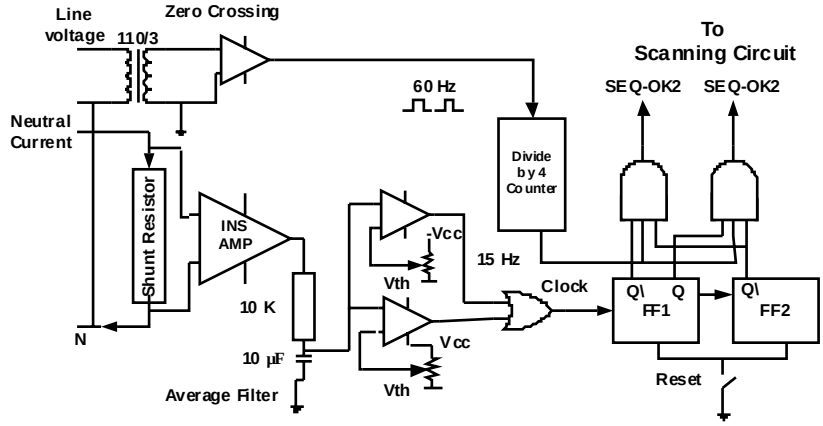

Fig. 2. Indication circuit.

most sophisticated part in the proposed scheme, which is composed of several counters, decoders and analog switches (Abou-Elela *et al.*, 1994; Abou-Elela *et al.*, 1998).

This paper is directed to overcome the disadvantages of the above scheme. Specifically, the redundant time consumed in the scanning of the trails. The new proposed scheme reduces the scanning time to less than 30% of the time required for scanning system proposed earlier (Abou-Elela *et al.*, 1994; Abou-Elela *et al.*, 1998). The scheme has also the following features:

- Simplicity.
- Programmability and flexibility.
- Built around a single chip.
- Pure digital scanning circuit.
- Built in self-generated firing pulses for testing purposes.
- Built in self-test routine.

II. The Principle of Operation

The principle of operation of the self-adjustment correction of the firing signals for the working thyristors depends on the scanning of all the possible connections between the six firing signals and the corresponding six gates for the working thyristors. The scanning process is stopped when all the six working thyristors are fired properly. The scanning process will be stopped by detecting the average value of the neutral current.

An indication circuit is developed and implemented for this purpose, as a part of the previous scanning scheme. It triggers and controls the scanning operation by generating the sequence okay pulses (SEQ-OK1 and SEQ-OK2) for positive and negative gates groups, respectively. The main task of the indication circuit is to sense the average value of the neutral current via a small series resistor in conjunction with an instrumentation amplifier and averaged with a low pass filter. Two comparators with positive and negative threshold voltages are used to trigger a simple logic circuit that in turn generates SEQ-OK1 and SEQ-OK2. These pulses are used to stop both positive and negative scanning circuits when the correct firing process has been achieved. Figure 2 depicts the circuit diagram of the indication circuit (Abou-Elela *et al.*, 1998).

In the previous work, as show in the scanning circuit in Fig. 2, is divided into two identical sections for positive and negative firing groups. It consists of six parallel channels of divide by six counter, (3-8) line decoder and six analog switches (Abou-Elela *et al.*, 1994; Abou-Elela *et al.*, 1998). The six channels are connected in cascade. By this configuration, all the available combinations are searched in a sequential straight forward manner using the six free running divide by six counters. To reduce the number of required scanning trails, the scan process are implemented in two successive stages, positive then negative groups, in this case, the total number of combinations is reduced to:

$$2 \times 6^3 = 432 \qquad \text{combinations.}$$

Hence, the maximum (worst case) scanning time is given by:

$$Tc = \frac{2 \times 6^3}{fc} \qquad \text{seconds}$$

where f_c is the clock frequency. For 60 Hz AC supply, $fc = f/4 = 15$ Hz. T_c of the worst case scanning time is 28.8 sec.

III. Scanning Scheme

In the previous scanning the searching counters go through the easiest normal counting mode, which is, the binary sequence counting, i.e. the counting sequence states will be (Abou-Elela *et al.*, 1998):
000000,000001,000010,…..,111100,111110,111111
This counting sequence configuration will let the scanning process checks all the counters states including the non-possible combinations and this will add a redundant states as far as the scanning time is concerned.

In the new scheme, the scanning process can be speeded up and a significant reduction in the scanning time can be achieved when the scanning binary counters are modified and reconfigured in such a way that the irrelevant counting states are by-passed. These irrelevant counting states the non-possible firing combinations, such as the non-occurred combinations where the same firing pulse is selected to trigger more than one thyristor are considered. In this case, the corresponding combination will be skipped during the scanning phase. To do so, the scanning counters must be reconfigured to be a non-binary and go only through the useful states by skipping the unused ones. This will disable the possibility of considering more than one thyristor is triggered by the same firing pulse. Therefore, the counting sequence must be modified to go only through the valid states. The implementation of this counting sequence is very complicated using of-the-shelf discrete conventional components. It requires additional logic circuit. However, this can be easily implemented and by using the Programmable Logic Devices (PLD), where the required counting sequence can be described by special programming software (MACHXL software manuals, 1996).

A further considerable reduction in the scanning time is achieved; when the search is done in two successive phases (positively then negatively triggered groups). If the search is started by the positive one, for example, the search is done within the group in two stages, first one is to select three positive firing pulses out of six and logical sequence is indicated in the flow chart for Fig. 3. This is in probability equivalent of finding the number of selections of r out of n objects and the order of selections being immaterial (Anthony *et al.*, 2002). This is in probability called the number of combinations of n things taken r at a time and it is denoted by ${}_nC_r$ or $\binom{n}{r}$ and given by:

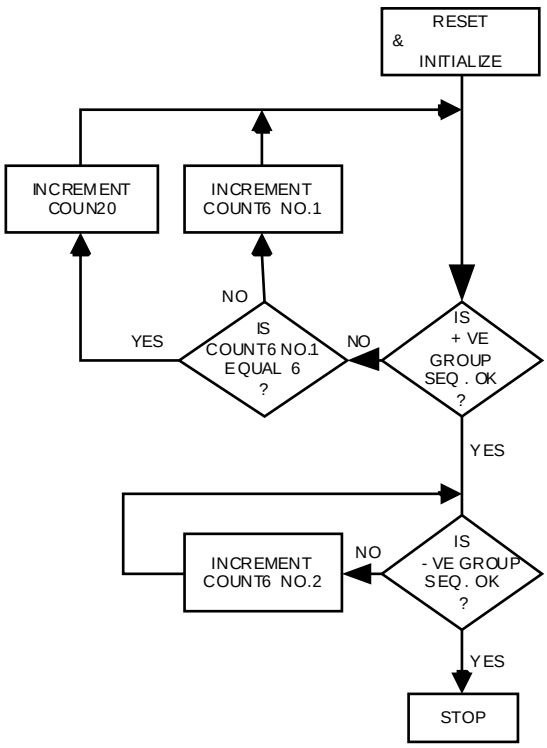

Fig. 3. Flow chart for the proposed scanning system.

Table 1. Possible combinations of firing pulses selection

No.	Positive group			Negative group		
	AG	BG	CG	DG	EG	FG
1	ANG-000	ANG-060	ANG-120	ANG-180	ANG-240	ANG-300
2	ANG-000	ANG-060	ANG-180	ANG-120	ANG-240	ANG-300
3	ANG-000	ANG-060	ANG-240	ANG-120	ANG-180	ANG-300
4	ANG-000	ANG-060	ANG-300	ANG-120	ANG-180	ANG-240
5	ANG-000	ANG-120	ANG-180	ANG-060	ANG-300	ANG-240
6	ANG-000	ANG-120	ANG-240	ANG-180	ANG-300	ANG-060
7	ANG-000	ANG-120	ANG-300	ANG-180	ANG-240	ANG-060
8	ANG-000	ANG-180	ANG-240	ANG-300	ANG-120	ANG-060
9	ANG-000	ANG-180	ANG-300	ANG-240	ANG-120	ANG-060
10	ANG-060	ANG-120	ANG-180	ANG-240	ANG-000	ANG-300
11	ANG-060	ANG-120	ANG-240	ANG-300	ANG-000	ANG-060
12	ANG-060	ANG-120	ANG-300	ANG-240	ANG-000	ANG-180
13	ANG-060	ANG-180	ANG-240	ANG-120	ANG-000	ANG-300
14	ANG-060	ANG-180	ANG-300	ANG-120	ANG-000	ANG-240
15	ANG-060	ANG-240	ANG-300	ANG-120	ANG-000	ANG-180
16	ANG-120	ANG-180	ANG-240	ANG-060	ANG-000	ANG-300
17	ANG-120	ANG-180	ANG-300	ANG-060	ANG-000	ANG-240
18	ANG-120	ANG-240	ANG-300	ANG-060	ANG-000	ANG-180
19	ANG-180	ANG-240	ANG-300	ANG-060	ANG-000	ANG-120
20	ANG-240	ANG-000	ANG-300	ANG-060	ANG-180	ANG-120

$$nCr = \frac{n!}{r!(n-r)!} \quad \text{combinations} \qquad (1)$$

In our case, when substituting in the above equation, where the number of objects is the positive and negative firing pulses which is equal to six, and the number of selections is 3. Thus, the number of combinations is given by:

$$nCr = \frac{n!}{r!(n-r)!} = \frac{6!}{3!(6-3)} = 20 \quad \text{combinations}$$

The possible combination is shown in Table 1. The firing pulses shown in Table 1 are denoted by ANG-000 to ANG-300.

Table 2. Firing pulses arrangement for the positive group (as shown in Fig. 4)

S12	S11	S10	XG	YG	ZG
0	0	0	AG	BG	CG
0	0	1	AG	CG	BG
0	1	0	BG	AG	CG
0	1	1	BG	CG	AG
1	0	0	CG	AG	BG
1	0	1	CG	BG	AG

The next stage is to rearrange and determine the possibility for the proper sequence of the firing pulses within the three already selected ones, this is simply performed by a number of trails given by:

$$3! = 6 \qquad \text{trails}$$

The different combinations are shown in Table 2. Therefore, the overall number of trails to search all the possible combinations in the positive group is equal to 20 x 6 = 120 trails. This represents the worst case to find the proper sequence for the positive group. Successively, when the positive group search is achieved and the proper firing pulses are assigned accordingly, then the second phase of the search for the negative one which is simply done by rearranging only the three remaining non-selected firing pulses by the positive group as shown in the Table 3, which requires only six trails. Hence, the total number of trails for the overall complete run is given by:

$$6 \times 20 + 6 = 126 \quad \text{trails}$$

Hence, the worst overall scanning time assuming 15 Hz scanning clock for 60 Hz line frequency is just:

$$t = \frac{126}{15} = 8.4 \qquad \text{seconds} \qquad (2)$$

This represents the total time required to scan the six different firing pulses and assign the proper ones for each of the six gates for the working thyristors.

Table 3. Firing pulses arrangement for the negative group (as shown in Fig. 4)

S22	S21	S20	UG	VG	WG
0	0	0	DG	EG	FG
0	0	1	DG	FG	EG
0	1	0	EG	DG	FG
0	1	1	EG	CG	DG
1	0	0	FG	DG	EG
1	0	1	FG	EG	DG

IV. Scanner Hardware Description

The scanner circuit is considered as the crucial unit and plays the major role in the new proposed scheme. Its significant task, as described earlier, is to scan all the possible combinations for the firing connections and decides to stop the scanning operation when the proper one is reached. As depicted in the simplified schematic diagram in Fig. 1, the scanner circuit works in conjunction with two secondary sub circuits, which are the indication and firing circuit. The firing circuit is responsible for generating the six different firing pulses required by the scanner circuit. The indication unit generates the control pulses to stop the scanning operation.

The scanner circuit is clocked by the line frequency (60 Hz) and receives the proper sequence indication pulses SEQ-OK1 and SEQ-OK2 for both positive and negative groups respectively. The scanner circuit output is the six firing pulses arranged in the proper sequence.

As illustrated in the detailed functional block diagram of Fig. 4, the new scanner hardware and the firing pulses circuit are built around a single chip programmable device (PLD). The scanner circuit consists of two overlapped subunits for positive and negative groups and is mainly composed of six different units:

- 2 divide by six counters.
- divide by 20 counter.
- 6 (5-3) decoders.
- 6 (6-1) multiplexers.
- 2 six states scanners.
- built-in self-generated firing angle pulses generator.

The squared up 60 Hz supply frequency is fed to a divide by four counter (CNT4) to generate a 15 Hz.

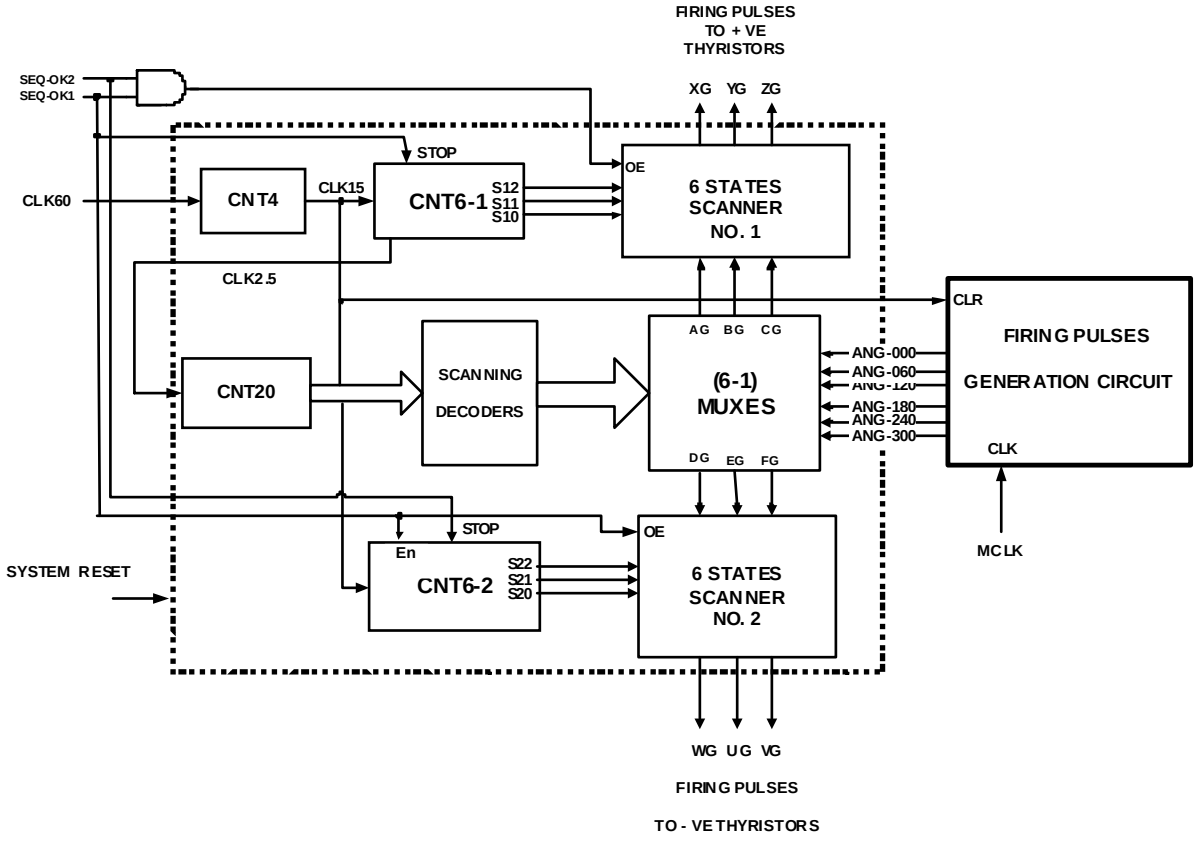

Fig. 4. Functional block diagram for the proposed scheme.

Clock (CLK15) is used as a master clock for the scanner circuit. The CLK15 triggers the positive group divide by six counter (CNT6-1) which in turn generates a 2.5 Hz clock (CLK2.5), and at the same time it produces six different states on its output lines (S_{10}, S_{11} and S_{12}). These lines are used as data selector for the positive six states scanner (No. 1) for firing pulses arrangements during the positive groups scanning phase.

The divide by 20 counter (CNT20) is clocked by CLK2.5 and its task is to produce 20 different combinations on its five output lines that can be decoded through the scanning decoder to implement the 20 different possibilities of scanning for the six firing pulses shown in Table 1. The decoder receives the five CNT20 output lines and generates six groups of three lines each, representing the data select inputs for the six of (6-1) multiplexers for firing pulses selection for both positive and negative groups. These decoders are simply behaved like a transformation look-up tables.

Table 4 represents the transformation table assigned for the positive gate denoted by AG. The tables for the other gates are developed in the same way.

When the proper sequence is achieved for the positive group, the negative group scanning on the remaining non-selected firing pulses works in the same manner as the positive phase using another divide by six counter (CNT6-2) in conjunction with six state scanner (No. 2).

During the scanning phase for the positive group, the SEQ-OK1 pulse generated by the indication circuit, as highlighted in the next section, goes high indicating that the proper sequence for the positive group is achieved. This pulse also is used to trigger the following:

- Stop the positive group counter CNT6-1 by forcing the count enable input to zero state.
- Enable the counting for the counter CNT6-2
- Enable the output of the negative firing angle pulses.

Finally, the process is stopped by the SEQ-OK2 pulse (generated by the indication circuit), when it goes high indicating that the proper sequence is fulfilled for both positive and negative sides. This pulse is also employed to disable the counting of the negative group counter CNT6-2.

A new run can be resumed once the SYSTEM RESET push-button switch is pressed. This switch will clear the contents of all the relevant counters and enable the output for the positive firing pulses side to begin a new run starting from the positive group then the negative one sequentially.

V. Firing Circuit

The built-in firing pulses generation circuit is composed of six identical units, but triggered by different signals to generate the firing pulses with the necessary phase shift. Each unit consists of two stage counters with some logic and connected in cascade. A (59.52 KHz) crystal oscillator is used as a master clock and fed to a divide by 16 counter to produce a 3720 Hz, then divided by 72 to get the firing angle pulse with a 5-degree resolution. This is desirable

Table 4. Transformation table assigned for the first positive gate

No.	CNT20 OUTPUT					Decoder Output			Firing Pulse
	C4	C3	C2	C1	C0				
0	0	0	0	0	0	0	0	0	ANG-000
1	0	0	0	0	1	0	0	0	ANG-000
2	0	0	0	1	0	0	0	0	ANG-000
3	0	0	0	1	1	0	0	0	ANG-000
4	0	0	1	0	0	0	0	0	ANG-000
5	0	0	1	0	1	0	0	0	ANG-000
6	0	0	1	1	0	0	0	0	ANG-000
7	0	0	1	1	1	0	0	0	ANG-000
8	0	1	0	0	0	0	0	0	ANG-000
9	0	1	0	0	1	0	0	1	ANG-060
10	0	1	0	1	0	0	0	1	ANG-060
11	0	1	0	1	1	0	0	1	ANG-060
12	0	1	1	0	0	0	0	1	ANG-060
13	0	1	1	0	1	0	0	1	ANG-060
14	0	1	1	1	0	0	0	1	ANG-060
15	0	1	1	1	1	0	1	0	ANG-120
16	1	0	0	0	0	0	1	0	ANG-120
17	1	0	0	0	1	0	1	0	ANG-120
18	1	0	0	1	0	1	0	0	ANG-180
19	1	0	0	1	1	1	0	1	ANG-240

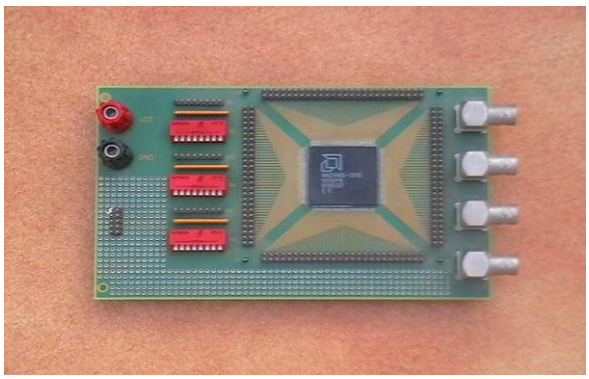

Fig. 5. Photograph for the PLD digital board.

because in some applications significantly different phenomena may take place within 5° range. The high frequency clock is used to minimize the firing pulse jitter. The above circuit configuration is repeated six times for producing the required six firing pulses shifted by 60 degrees from each other. Since the circuit design is built around a PLD chip that has a configurable design, it provides flexibility in the future to modify the design to any desired configuration.

VI. Experimental Verification

A) Scanner circuit testing

The hardware subunits for the scanner, firing angle generator and the self test routine have been developed. It is down loaded in a single PLD chip using MACHXL software package that is provided by the manufacturer for programming the employed MACH chip (*MACH445).* It can be reprogrammed on board, using the PC via the serial port interface. Figure 5 depicts the photograph for the PLD digital board. The design has been divided in several modules that can be simulated during the design phase individually. Figure 6 shows a sample of the print out for some of the tested relevant signals during the development phase which are displayed using the logic analyzer.

B) Experimental work

The complete set-up for the prototype of the proposed circuity has been tested. The typical waveforms for the phase and neutral currents are obtained under different firing conditions. Figure 7(a) gives the corresponding currents when only one thyristor is properly fired, whereas the other two thyristors are not fired, Figure 7(b) shows another firing condition when just one thyristor is properly fired where the other two thyristors are not. Figure 7(c) represents the case where all the thyristors are incorrectly fired. Figure 8 shows different configurations, when two thyristors are fired where the third one is either unfired (Fig. 8(a)) or improperly fired (Fig. 8(b)). Finally, Fig. 9 depicts the correct firing operation. To test the validity and

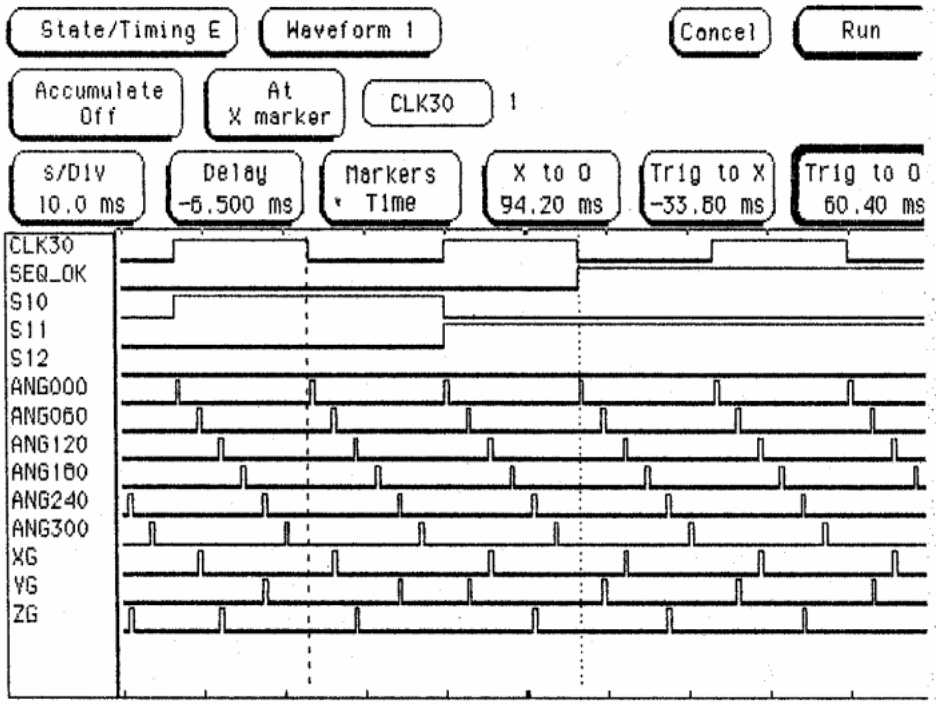

Fig. 6. A sample of the print out for some signals displayed using logic analyzer.

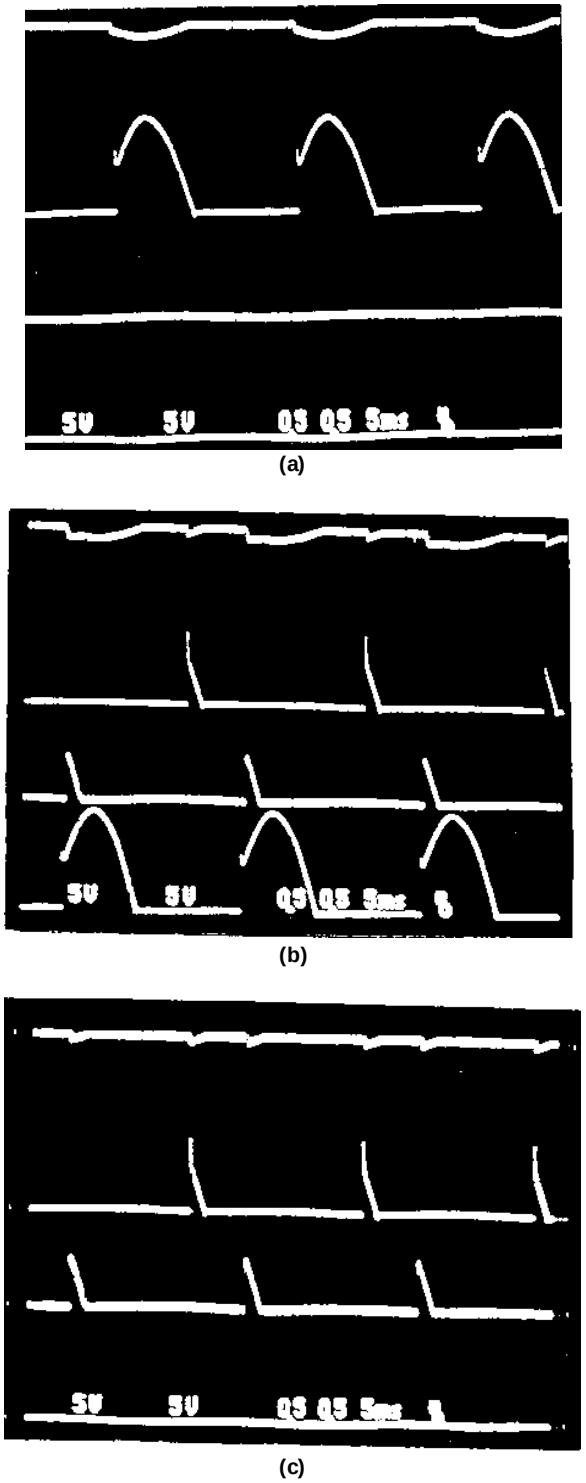

Fig. 7. Waveform of the line and neutral currents when: (a) only one thyristor is properly fired while the others are not fired; (b) only one thyristor is properly fired while the others are not properly fired; (c) all thyristors are properly fired.

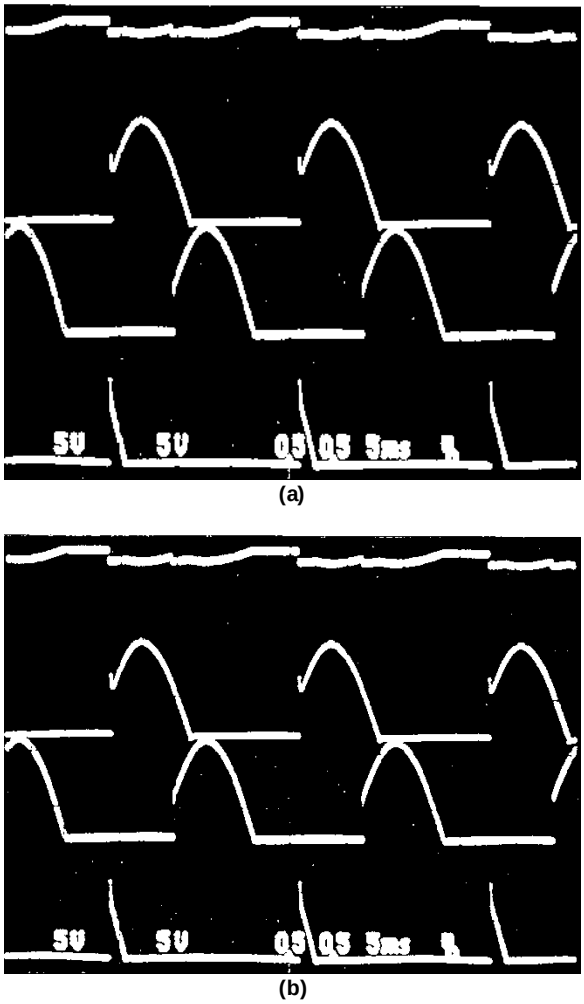

Fig. 8. Waveform of the line and neutral currents when two thyristors are properly fired while the third one is: (a) unfired; (b) improperly fired.

feasibility of the proposed circuit operation, the average value of the neutral current is recorded during the scanning of the possible configuration of the scanning circuit. The waveforms are recorded using storage oscilloscope. Figure 10 shows the recorded waveforms. From the above tests, one may conclude the following remarks:

- The scanning circuit is able to scan all the possible combiations within the time estimated in Eq. (2), as a worst case condition.
- The average value of the neutral current does not exceed 2/3 of its maximum value except for the proper firing condition.
- The scanning circuit stops its operation as soon as the correct configuration is satisfied.

Different tests that are carried out on the set-up proved that the proposed scanning can meet the

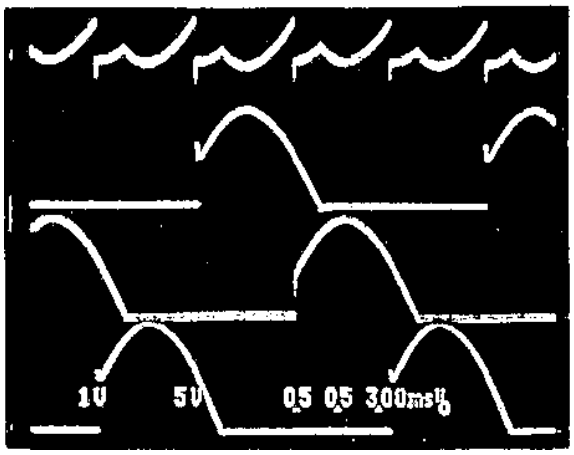

Fig. 9. Waveform of the line and neutral currents when all thyristors are properly fired.

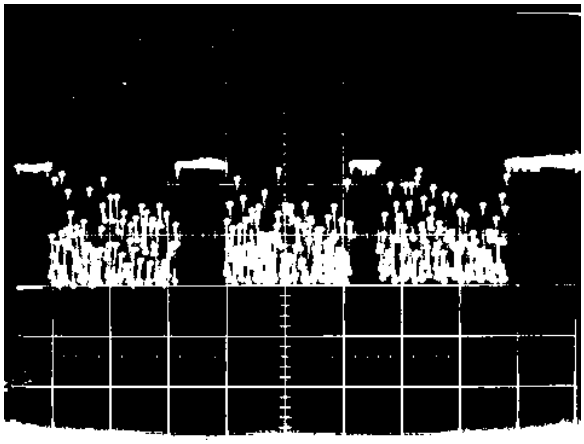

Fig. 10. Variation of the average value of the neutral current versus time during scanning operation.

scanning speed to correct the firing pulses and the process stops within a maximum time of 8.4 seconds.

From the above results, it may be concluded that the circuit operation confirms our requirements, and this simple scheme is suitable to make the circuit insensitive for any phase or sequence alterations. The system is also capable of detecting the faulty thyristors and can determine the phases sequence too.

VII. Conclusion

In this work, a novel automatic fast scanning scheme is proposed for phase and sequence adjustments. The proposed scheme can be applied to any firing circuit working in a four-wire AC voltage controller. The complete scanning circuit with the firing pulses generation is implemented on a single chip PLD. It has the following significant advantages over the circuits published earlier:

- Three times faster.
- Provides phase sequence indication.
- Simplicity and reliability.
- Programmability and flexibility.
- Built-in self-generated firing pulses.
- Self-test capabilities for circuit diagnoses.

The experimental tests carried out verify the validity and feasibility of the proposed system. This enables the firing circuit to automatically adjust itself against any phase and/or sequence alterations in short time, which eliminates the manual adjustment usually needed in such cases, in addition to avoiding any risk in circuitry. The worst case response time of the scheme to attain correct firing adjustment is 8.4 seconds for a line frequency of 60 Hz.

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دائرة إشعال ثلاثية الطور سريعة وذاتية الضبط معتمدة على الشرائح البرمجية لتطبيقات التحكم

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الرياض ، المملكة العربية السعودية

(قدم للنشر في ٢٠٠٧/٠٣/٢٠م ؛ وقبل للنشر في ٢٠٠٧/١٠/٢٤م)

ملخص البحث. تشرح هذه المقالة طريقة آلية بسيطة ومرنة وسريعة لتزويد الثايروستورات بنبضات الإشعال الصحيحة بغض النظر عن أخطاء التوصيل الناتجة في تطبيقات أنظمة التحكم ثلاثية الطور وذات الأربعة أسلاك. هذه الطريقة المقترحة والمبنية باستخدام الأجهزة القابلة للبرمجة بإمكانها ضبط نفسها في حالة عدم التوصيل أو عكس ترتيب نبضات الإشعال في زمن لا يتجاوز ٨.٤ من الألف من الثانية. بالإضافة إلى ما سبق فإن النظام بمقدوره تحديد الثايروستورات التالفة وكذلك توليد الاختبارات التشخيصية ، وتؤكد النتائج المعملية صحة مبدأ التشغيل.