J. King Saud Univ., Vol. 16, *Science* (2), pp. 77-85, Riyadh (A.H. 1424/2004)

Structural and Electrical Properties of Au/Si:H diodes

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(Received on 23/6/1422H; accepted for publication on 22/8/1423H)

Abstract. N-type <100> crystalline silicon wafers were used as a substrate for a-Si:H film deposited. Aluminum was evaporated onto device quality a-Si:H films deposited in an ultra high vacuum plasma enhanced chemical vapor deposition (PECVD) system. The Al/a-Si:H samples were annealed in the range of 50-400^{0}C, for 30minutes. XRD analysis showed a very good polycrystalline of the interacted film at 350^{0}C. Schottky barriers were made by vacuum evaporation of a gold onto the a-Si:H surfaces after removing the Al by a standard etching solution. Current- voltage characteristics (J-V) characteristics and capacitance-voltage measurements (C-V) were carried out as a function of temperature annealing of Al/a-Si:H substrate. The ideality factor, barrier height and carrier concentration were calculated.

Introduction

Recently hydrogenated silicon has received increasing attention because of its wide range of applicability in large area electronics including thin film transistor, solar cells and image sensors [1,2]. Moreover, it has been reported that at 150 ^{0}C Al starts to interact with a-Si:H [3-6] and a-Si [7] films yielding crystallized silicon on these films surface. Crystallization of a-Si:H in contact with different metals during annealing at relatively low temperature has been achieved [5,8]. Changes in Al/c-Si contact properties during sintering have been studied extensively for the last few decades. It has been found that n-type c-Si under Al contacts becomes heavily counter doped (10^{18} cm^{-3}) by Al at 500 ^{0}C [9]. However, for the case of Al/a-Si:H, the interaction temperature is much lower, starting at 170 ^{0}C [3]. On the other hand, low temperature, metal induced crystallization of a-Si:H is not well understood and a complete understanding of the mechanism involved has not yet been achieved. Only a few models have been reported to explain the catalytic behavior of a metallic film during crystallization of amorphous film during annealing at low temperature [3,10]. Some of these researchers investigated the interact of Ni, Au, Ag and Al [11, p. 139]. Moreover, the effects of the annealing during the crystallization process on the solar cells performance have not been intensively studied.

In this article, the interaction of Al with a-Si:H film was studied through the XRD as a function of temperature annealing. Schottky barriers were fabricated on a noncrystalline and crystalline Si films and the ideality factor and the barrier height were determined through J-V characteristics and capacitance voltage (C-V) measurements.

Experimental Procedures

N-type <100> crystalline silicon wafers were used as substrates for a-Si:H film deposition. The silicon substrates were first cleaned using standard cleaning methods. The a-Si:H were deposited on the substrate using a ultra high vacuum(UHV) plasma enhanced chemical vapor deposition (PECVD) system. During the deposition, the temperature, pressure and power density were 250 ^{0}C, 500 mtorr and 50mW/cm^2, respectively. A phosphorous concentration of 1% was used for all films. After the deposition, the samples were allowed to cool to room temperature in vacuum. The chamber was then filled with dry nitrogen and the samples were immediately transferred to a thermal evaporation system where an Al film of approximately 3000^{0}A was deposited at room temperature. The samples were then annealed at different temperature (0-400 ^{0}C) for 30 minutes. In order to observe the crystallization of the a-Si:H, the Al surface was etched from the samples after the annealing process. A conventional Al etching solution (85 parts phosphoric acid, 5 parts acetic acid, 5 parts nitric acid, 5 parts de-ionized water at 50 ^{0}C was used. A gold dot was evaporated to the substrates to form Schottky diodes.

X-ray diffractometry was used to determine the lattice and structure of Si film. This was done using a Siemens D5000 with Cu Kα radiation of average wavelength 1.54056^{0}A. It was operated with target voltage and current 30kV and 20mA respectively. The diffraction patterns were from 2θ = 0 to 2θ = 80^0. Dark current-voltage (J-V) characteristics were made and capacitance-voltage (C-V) measurements were obtained (at 1MHz) using a Model 410 Princeton Applied Research Capacitance bridge. The measurements of the dark current-voltage characteristics were carried out point by point. During these measurements, the samples were covered to keep them in the dark.

Result and Discussions

In order to observe the crystallization of the a-Si:H, the Al surface was etched from the samples after the annealing process. Figure 1 shows the X-ray diffraction spectra of the Al/a-Si:H films after annealing at 250, 300, 350, and 400 ^{0}C for 30 minutes. A four crystalline silicon peaks are clearly present in all films, which indicates a good polycrystalline films. The crystalline silicon peaks at d=1.357 (400); d=1.631 (311), d=1.904 (220) and d=3.131 (111) appear in the Al/a-Si:H polycrystalline silicon annealed at different temperature for 30 minutes. The XRD intensity of these films increases with annealing temperature. When the samples were annealed at 50, 100, 150, and 200 ^{0}C for 30 minutes, no crystalline silicon peaks were observed. It is clear that the solid phase crystallization temperature can be obtained above 200 ^{0}C. Good polycrystalline films were observed for annealing at relatively low temperature by other researchers [12,13]. In their proposed model for metal-assisted crystallization, the metal-rich silicide formed during the initial stage of the interaction is expected to reject all Al metal during crystallization [3]. The possibility of some of the rejected Al segregating at the grain boundaries is thus ruled out by XRD measurement results.

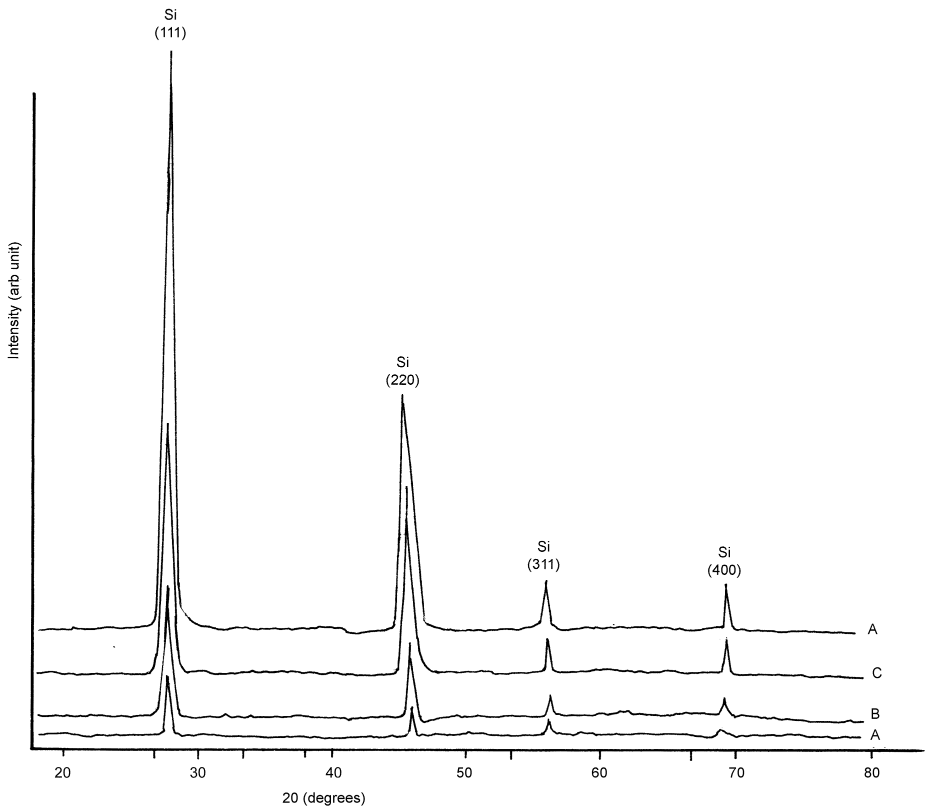

Fig. 1. X-ray diffraction spectra of a-Si:H films annealed at (a) 250^{0}C; (b) 300^{0}C; (c) 350^{0}C and (d) 400^{0}C for 30 minutes.

Figure 2 shows the J-V characteristics of gold silicon diodes. Two graphs were shown in this figure. Graph A represents a Schottky diodes fabricated on a silicon films, which annealed at 200 ^{0}C whereas graph B represents a Schottky diodes fabricated on a silicon films, which annealed at 350 ^{0}C. It is clear that annealing at 350 ^{0}C for 30 minutes of the substrate shows a rectifying with a small reverse bias leakage current. As is evident from Fig. 2 the conductivity of samples A was low. It is known that annealing of the substrate at 200 ^{0}C for long time above 10 hours leads to a low conductivity [12].

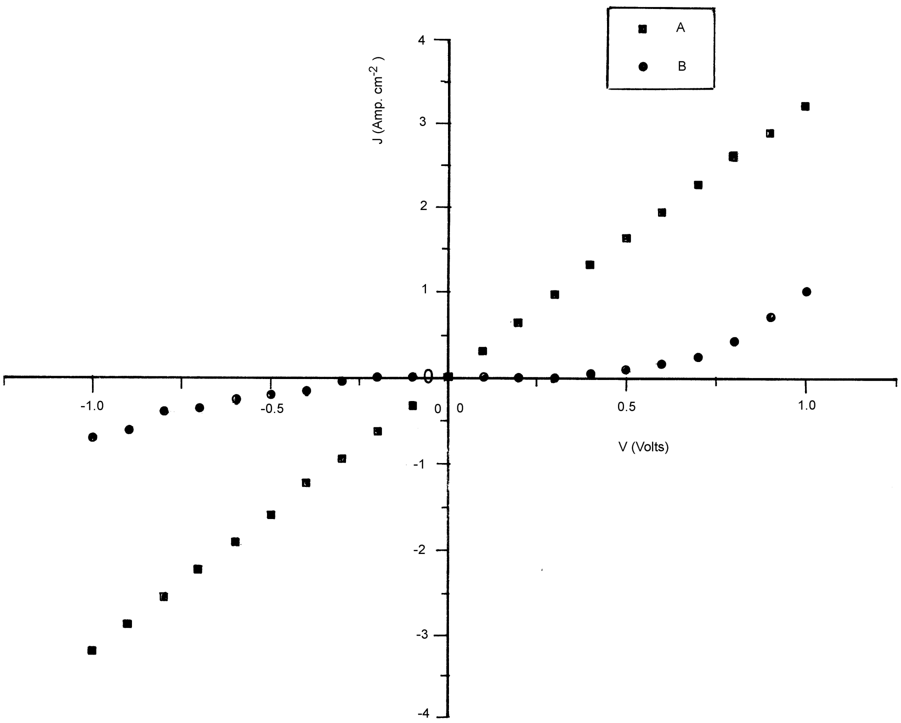

Fig. 2. Dark current-voltage characteristics (J-V) for Au-Si:H Schottky diodes formed on an a-Si:H substrates after annealed at (A) 200^{0}C and (B) 350^{0}C.

Figure 3 shows a semilogarithmic plot of J-V characteristics measured for gold-silicon diodes for the A and B devices. The current forward density, J, calculated by thermionic emission theory, is given by [14];

$$J=J_0\,[\exp qV/kT -1] \tag{1}$$

Where,

$$J_0 = A^* T^2 \exp [\ -q\varnothing_B /kT\ ] \tag{2}$$

is the saturation current density in the Schottky diode extrapolated to V=0, $\mathbf{A^*}$ is the modified Richardson constant (112A.cm^{-2}K^{-2} for n-type silicon) [15], V the bias voltage, q the electric charge, k the Boltzmann constant and T the temperature. The ideality factor n, is introduced into the formed current density expression for Schottky diodes, where the slope of the forward current density of the Schottky diodes is less than q/kT,

$$J=J_0\,[\,\exp(qV/nkT)-1]\tag{3}$$

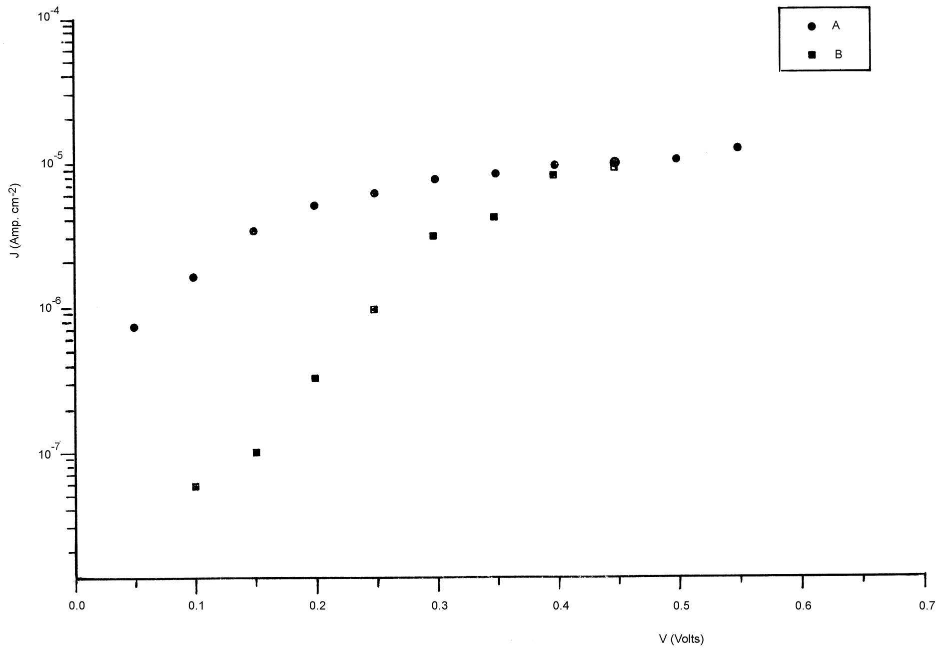

Fig. 3. The forward current versus forward voltage for Au-Si:H Schottky diodes formed on an a-Si:H substrates after annealed at (A) 200^{0}C and (B) 350^{0}C.

The ideality factor (n) was found to be 1.16 for devices A (the substrate annealed at 200 ^{0}C) and 1.92 for devices B (the substrate annealed at 350 ^{0}C). An ideality factor of about 1 proves that thermionic emission is the dominant mechanism of the charge transport. The barrier height ϕ_B can be calculated from Fig. 3 under the assumption validity of the thermionic emission theory of the Schottky diode current. By using equation 2 the value of the barrier height ϕ_B of B devices was found to be 0.61eV whereas 0.42eV was obtained for devices A. The value of devices A agrees well with the values reported by Simeonov and Kafedjiislca [16] where a good comparison of the values of the barriers height with a model of inhomogeneous Schottky barriers is presented.

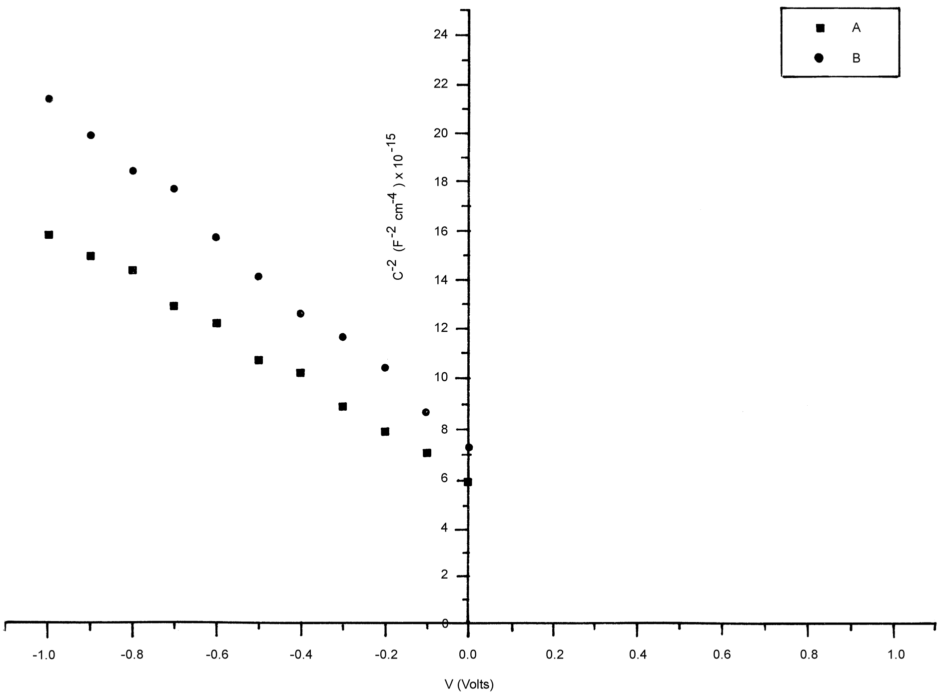

Fig. 4. C^{-2} versus the applied voltage for Au-Si:H Schottky diodes formed on an a-Si:H substrates after annealed at (A) 200^{0}C and (B) 350^{0}C.

Plot of $1/C^2$ against the applied voltage for the Schottky diodes for devices A and B are given in figure 4. These graphs, as expected [14], are straight lines with an intercept V_d on the x-axis. The barrier height was found to be 0.709eV for B devices and 0.490eV for A devices. The values of barrier height found from current voltage characteristics are sometimes in disagreement with those obtained from capacitance voltage measurements according to Goodman [17] and Cowley and Heffiner [18]. The donor concentration was calculated from Fig. 4 and it was found to be $6x19^{15}$ cm^{-3} and $0.5x10^{15}$ $cm^{-3}$for devices B and A receptively. The intersection of the extrapolated $1/C^2$ plots with the voltage axis, the diffusion voltage, are 0.52V and 0.61V for devices B and A respectively. Those devices fabricated on noncrystalline or semicrystalline silicon (the substrate annealed at 200 ^{0}C) will have a high density of interface state. Such high density could lock the top of the barrier relative to the Fermi level since the forward-current conduction mechanisms vary considerably depending on the density of surface state. For devices fabricated on crystalline silicon (the substrate annealed at 350 ^{0}C) will result in relatively low interface state densities, so the electron surmounting the potential barrier will tunnel through the interfacial layer.

Conclusion

A-Si:H film was deposited in an ultrahigh vacuum plasma-enhanced chemical vapor deposition (PECVD). A good polycrystallinity was obtained after annealing the Al/a-Si:H films at relatively low temperature through the XRD studies. Electrical properties of a Schotkky diodes (Au/Si:H) formed on a different structure of the silicon substrate at different temperature were carried out. The ideality factor, n, barrier height, $\phi_{B,}$ and donor concentration N_d was calculated as a function of annealing temperature through the current-voltage characteristics and capacitance voltage measurement. It is found, in this study, that annealing at 350 ^{0}C for 30 minutes of the substrate shows a rectifying with a small reverse bias leakage current.

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الخواص التركيبية والكهربائية لوصلة Au/Si:H

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(قدم للنشر في ٥/٧/١٤٢٢هـ ؛ قبل للنشر في ١٦/٧/١٤٢٣هـ)

ملخص البحث. استخدمت شرائح السليكون المتبلور كقاعدة لترسيب السليكون المهدرج غير المتبلور a-Si:H.تم تبخير a-Si:H بواسطة طريقة الترسيب الكيميائي البخاري (PECVD) ومن ثم تبخير الألومنيوم فوق هذه الطبقة. تم تسخين العينات عند درجات تتراوح من ٥٠ إلى ٤٠٠ ْم. بينت دراسات الأشعة السينية أنه قد حدث تبلور للسيليكون غير المتبلور عند درجه حرارة٣٥٠ ْم. تم تكوين وصلة الشوتكي بواسطة تبخير طبقة من الذهب فوق a-Si:H بعد إزالة الألومنيوم . تم قياس خواص الجهد - التيار و الجهد - السعة كدالة في درجه حرارة التسخين لـ Al/a-Si:H . تم حساب معامل المثالية و ارتفاع الحاجز الجهدي وكثافة حاملات الشحنة لتلك العينات.